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Harmonics Control By Using dSPACE With Multilevel Inverter

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Abstract — A multilayer inverter is used for highvoltage and high power applications. A Multilevel Inverter's output can have a higher number of levels. As the output level is increased, the harmonics are significantly decreased. This work describes the open loop control modelling and implementation of a three-level Diode Clamped Multilevel Inverter on the dSPACE DS1104controller platform. Using a dSPACE controller to construct a three-level Diode Clamped MLI and balancing the Diode Clamped MLI reduces output voltage distortion.

***Keywords*— dSPACE ;*Sinusoidal pulse;* multilevelinverter; Sinusoidal pulse width Modulation;**

INTRODUCTION

An electronic device or circuitry that converts direct current (DC) to alternating current (AC) is known as a power inverter or inverter (AC). The design of the specific device or circuitry determines the input voltage, output voltage and frequency, and overall power handling. The inverter does not generate any electricity; instead, the DC source provides it. For highvoltage and high power applications, multilevel inverters have become a well-established technology. Variable speed drives, power compensation, rolling mills, and renewable energy applications are all usingthe Three-Level Diode Clamped Multilevel Inverter (DCMLI). The purpose ofutilising diodes in DCMLI is to reduce the voltage stress on power components. The output voltage quality of the DCMLI is higher, with lower harmonic distortion, lower voltage stress across switches, and almost sinusoidal output waveform creation [3]. To lower the total harmonic load to avoid total harmonic distortion (THD) in output voltage, the potential across each dc-bus capacitor must be kept at half of the total supply voltage. The simulation utilising dSPACE and Matlab/Simulinksimulation software package, as well as the implementation in the DCMLI hardware kit, are the two primary aspects of this project.

To observe the output characteristics of each converter, the analysis and simulation would be carried out using dSPACE and Matlab/Simulink (R2010a) simulation tools. The project's major goal is to use dSPACE to generate carrier-based PWM signals with varied modulation indexes for DCMLI and to regulate DCMLI in real time.

In Fig.1. A dSPACE-based Master I/O card is used to record the controller's PWM signals. The times of rising and falling transitions are collected and passed to the DCMLI model after capturing PWM signals with a dSPACE-based card. To employ transition times, a particular DCMLI model, in this case a Real Time- EVENTS time-stamped inverter model [4], must be used, which implements interpolation for fixed-step simulation of voltage source inverters and PWM generation units.

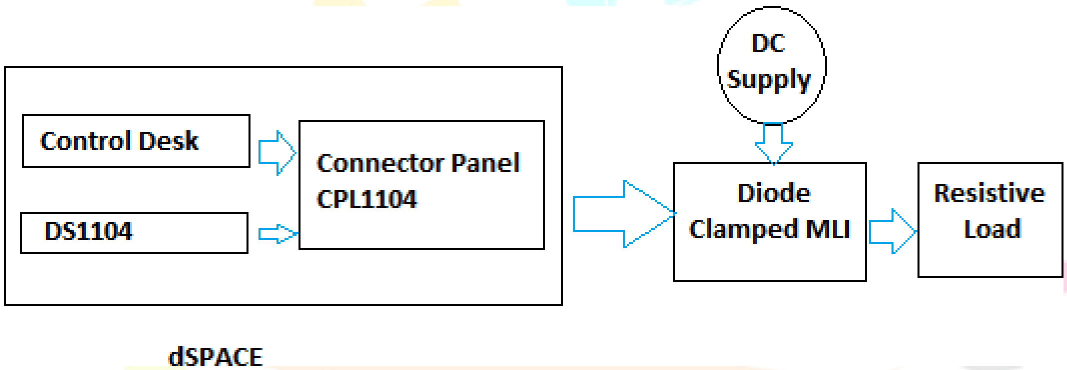


Fig.1. Block diagram

It is feasible to avoid the jitter problem observed when modelling switching converters at a large fixed time-step and related non- characteristic harmonics and anomalies by employing a dSPACE-based I/O board to capture PWM gate signals, as well as a time-stamped, interpolated inverter model.

DIODE CLAMPED MULTILEVELINVERTER

Utility interface systems and motor drives both benefit from multilevel converters. The THD of the output voltage is low, and the efficiency and power factor are good. They can handle high-voltage and high-current loads. Multilevel inverters used as rectifiers to convert ac to dc have a power factor that is near to unity. When the converters are in charge mode (rectification) or drivemode (inversion), there is no charge imbalance problem,and no EMI problemoccurs.

The diode-clamped inverter provides multiple voltagelevels through connection of the phases to a series bank of capacitors where, (m-level) inverter (DCMLI) typically consists of (m-1) capacitors on the dc bus and produces m-levels on the phase voltage. For a DC link voltage the voltage level of each capacitor is charged to for NPC. Due to the connections of the clamping diodes, the voltage stressacross the switching devices [5] is limited to one capacitor voltage level. Therefore, by increasing the number of voltage levels, the voltage stress across the semiconductor switches in this multilevel structure can be reduced significantly. Because of industrial developments over the past severalyears, the three-level inverter is now used extensively in industry applications. Fig.2. shows the structure of the three-level diode-clamped inverter, and Table I give the switching sequences to generate the three- level output voltage for phase "A."

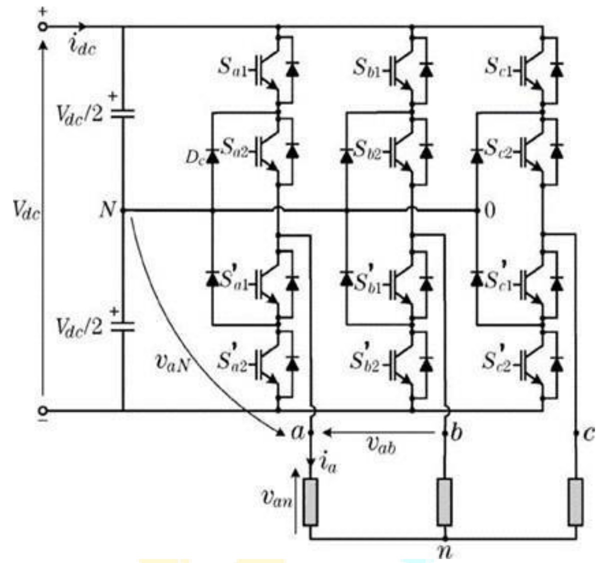


Fig.2. Structure of three-phase three-level diode-clamped inverter

SWITCHING STATES OF 3 LEVEL DIODE-CLAMPED INVERTER FOR PHASE A

Clamped Inverter

S. No	Switching States Sa1	Sa2	S'a1	S'a2	Switching States	Output Phase Voltage (Vao)
1	1	1	0	0	+	+(V/2)
2	0	1	1	0	0	0
3	0	0	1	1	-	-(V/2)

The switching states of the switches in the DCMLI inverter are represented by the switching states shownin table I. „P" indicates that the upper two switches inleg A are ON, and the inverter terminal voltage, whichis the voltage at terminal A with respect to neutral point O, is +E, whereas „n" indicates that the lower two switches conduct, resulting in -E. The inner two switches S2 and S3 are ON and are clamped to zero by the clamping diodes in the switching state "O." Theharmonic content is low enough to obviate the requirement for filters when the number of levels is high enough. Because all devices are switched at the fundamental frequency and the control approach is simple, DCMLI inverters have a high efficiency.

SIMULATION AND REAL TIME IMPLEMENTATION

The Sinusoidal PWM approach is more versatile and easy than the Space-vector method. Only one modulating sinusoidal signal is used in the Sinusoidal PWM technique, which employs two triangular carrier signals. The carriers are arrangedsuch that the bands they occupy are continuous and have the same frequency and peak to peak amplitude. The carrier set's zero reference is located in the middle. The modulating signal is a frequency and amplitude sinusoid. Each carrier iscompared against the modulating signal at every time. Each comparison returns a positive result ifthe modulating signal is bigger than the triangle carrier in the first half of the fundamental period, and a negative result if the modulating signal is lower in the second half of the fundamental period. zero otherwise.

The voltage level necessary at the inverter's output terminal is calculated by adding the results.This type of PWM has the advantages of being easily expandable to a large number of levels, being simple to construct, and accurately distributing switching signals to minimise switching losses and mitigate imbalanced dc sources. The PWM circuit for generating the gating signals for the multilevel inverter switches is shown in Figure 3. Two carriers are created and compared to a set of three sinusoidal reference waveforms at each time to operate a three phase multilayer inverter with a three-level output voltage. There is one carrier wave above and one carrier wave below the zero reference. These carriers have the same frequency, amplitude, andphase, but their dc offset is different, allowing them to occupy adjacent bands. The waveform of the sine-triangle junction is seen in Figure 4. SPWM control was achieved by combining two carriers with a modulation signal.

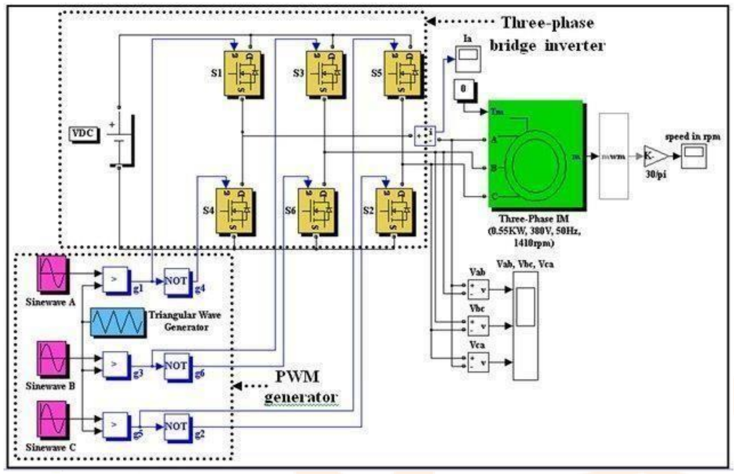


Fig.3.Simulation Diagram of three phase Sine PWM

Fig.4. Gate pulses for leg A switches.

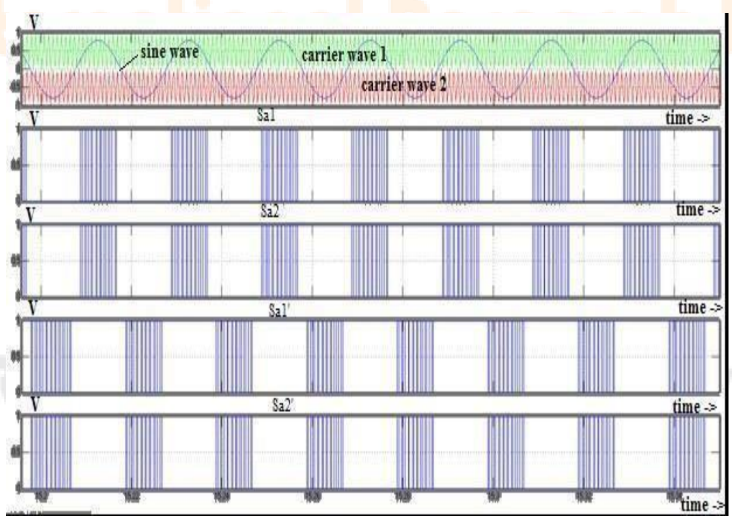


Fig.4. Gate pulses for leg A switches.

Fig.5. shows a simulated representation of the full circuit.The three-phase, three-level Diode ClampedMLI controllercircuit. The circuit is fed 12 pulses generated by a three- phase Sine PWM.

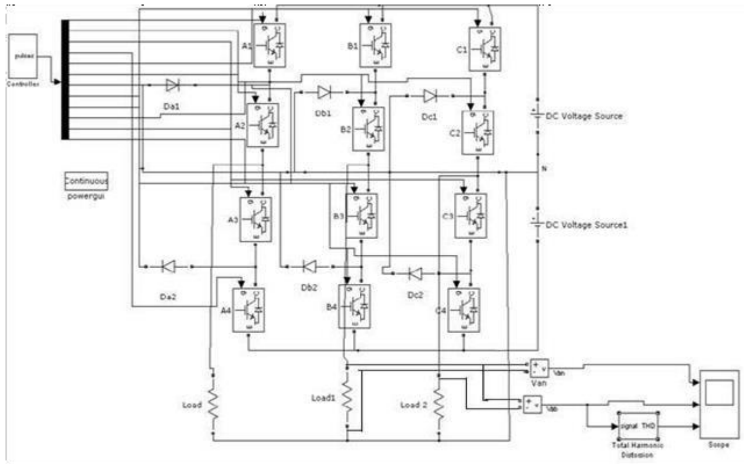


Fig.5. Simulated circuit

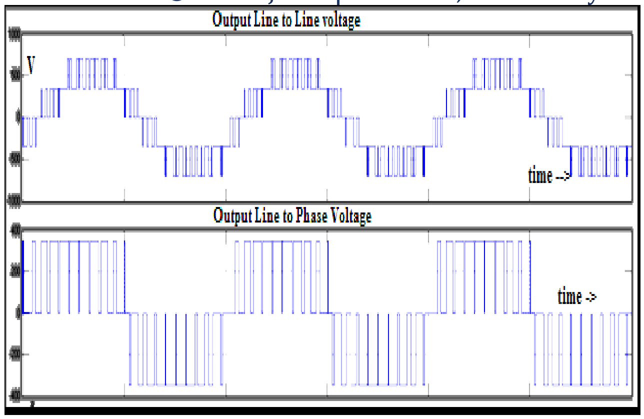


Fig.6. Output Voltages Of three phase sine PWMfor Diode Clamped MLI

SIMULATION OF THREE LEVEL DIODECLAMPED INVERTER USING DSPACE

The dSPACE control platform makes programming easier by providing a library blockset and allowing control algorithms to execute on the CPU and on-chip peripherals. In the hardware section, open loop simulation with real-time simulation implementation has been described. This is accomplished with the help ofa digital signal processor controller. To generate pulses, a dSPACE and MATLAB interface is being developed. The DS 1104 is used to generate PWM using the Sinusoidal PWM approach. Fig 7 depicts the essential componentsor modules that must be implemented. The control method may be executed on the processor, which is a 64-bit floating point MPC8240 processor with a PPC603e core and on-chip peripherals, thanks to the interface between MATLAB/Simulink and dSPACE DS1104 To create the needed 12 bits of data, themaster bit I/O is employed. The master bit I/O isutilised to create the 12 gate pulses that are required.

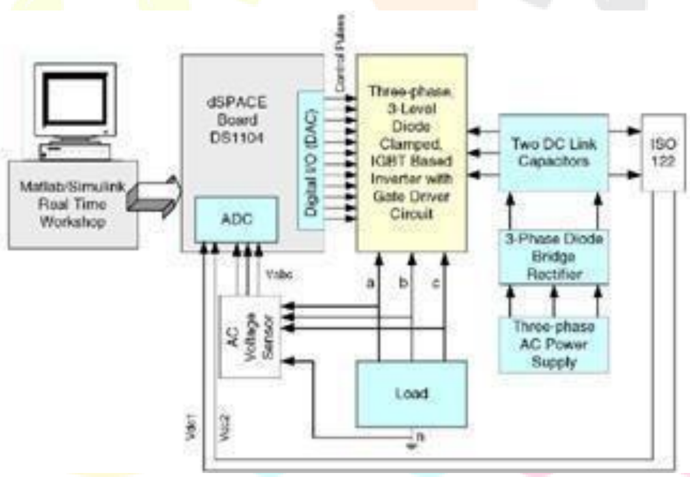
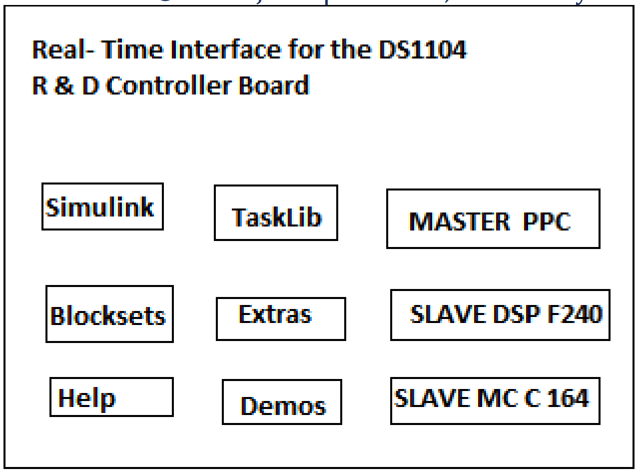
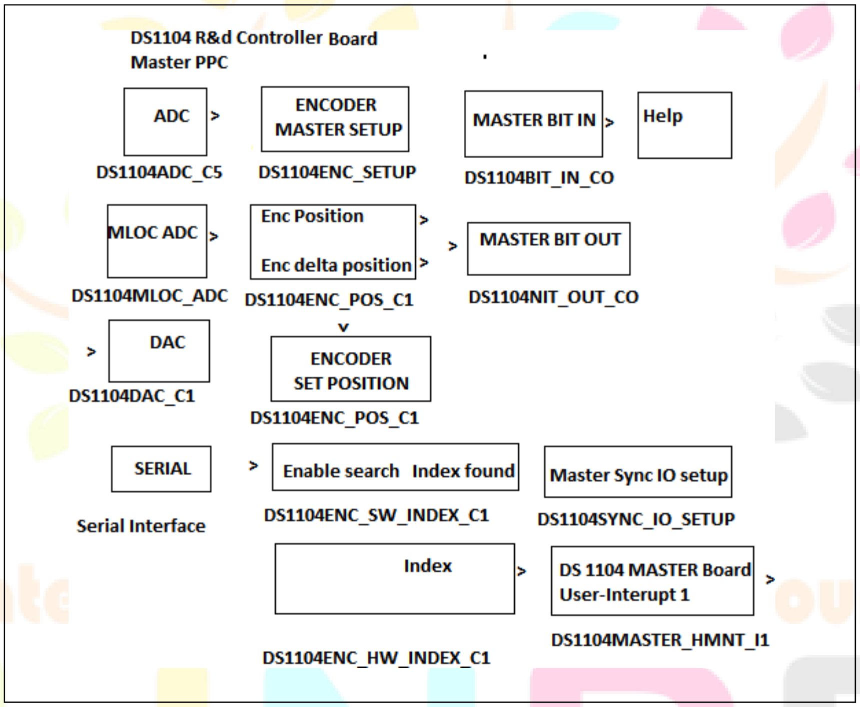


Fig.7. Block Diagram of dSPACE-DS1104 based

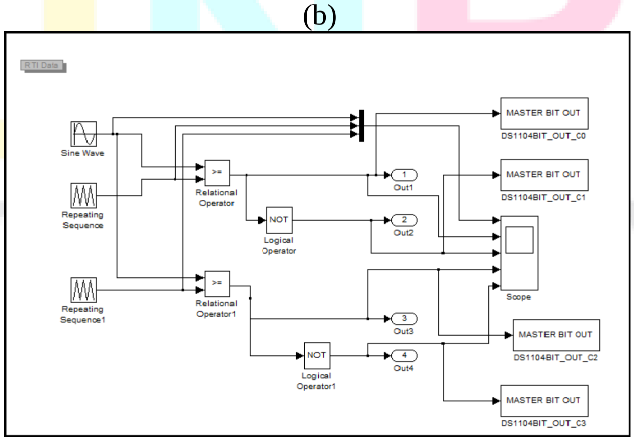
Three-Phase 3 Level Diode Clamped MLI Experimental Setup



(a)



(b)



(c)

Fig.8. (a) Real-Time Interface (RTI) DS1104Library block (b) RTI library Master PPC block (c) Simulink model for Pulse Generation inDiode Clamped Inverter(Phase A)

The Fig.8 (a) shows Real Time Interface (RTI) for DS1104 R & D controller boardopened in MATLAB. From this RTI Board library, Master PPC is selected and opened. From the window opened shown in Fig.8 (b) Master Bit out block is used in the pulse generation circuitry for the three level Diode Clamped inverter. The Fig.8(c) shows the simulink model for the pulse generation of three level Diode- Clamped inverter for PhaseA.

Fig.9. shows pulses generated using dSPACE hardware in Cathode Ray Oscilloscope (CRO)for phase-A. Phase-A has a single sinusoidal signal and two comparator to generate 4 pulseswith carrier frequency 1050 Hz and sine signalis the reference signal with 50 Hz. In this figurepulses are generated for MI=0.8.

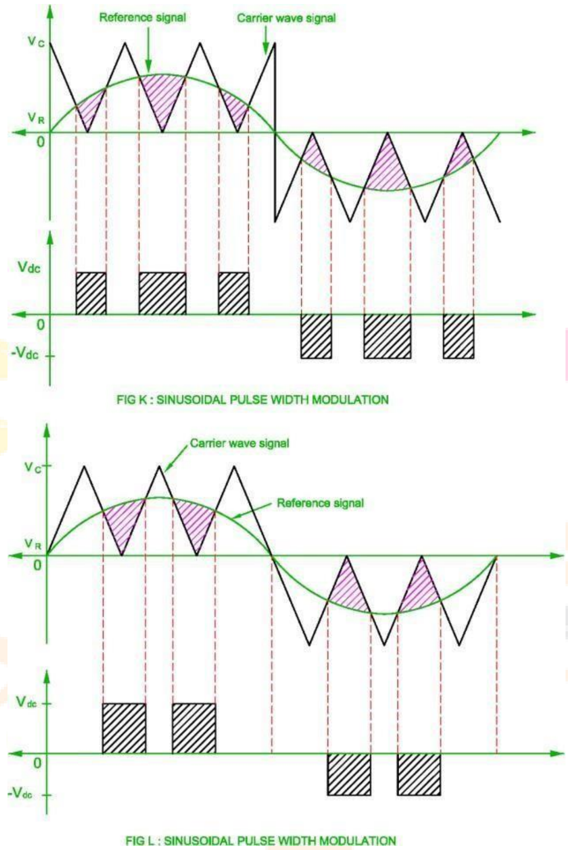


Fig.9. PWM pulses for the devices in phase-A

CONCLUSION

The three-level diode clamped MLI is controlled in real timeusing dSPACE software, which generates carrier-based PWM signals for various modulation indexes for Diode Clamped MLI. For three levels diode clamped MLI, only open loop implementation is presented. This project uses three-phase sine PWM to create 12 pulses. Using diode clamped MLI, this approach generates three levels. The modulation index of 12 pulses is examined in DSO. dSPACE is used to create a three-level, three-phase Diode Clamped Multilevel inverter. Only the open loop is available here. The Real Time Interface (RTI) between Matlab/Simulink and the dSPACE DS1104 is used to create the pulse generation technique for triggering inverter switches on hardware.

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