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LOW POWER OPERATIONAL AMPLIFIER DESIGN

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Abstract: The operational amplifier is one of the most popular building blocks in the design of integrated circuits today. The numerous applications are not restricted to just signal processing and filtering but it is widely used in the applications such as analog to digital conversion, biomedical instrumentation, communication systems and many more. With the advent in portable, battery operated electronic devices; there is a constant need for minimum power consumption, low power consuming operational amplifiers which can maximize the performance.

The architecture addresses the typical design limitations of conventional CMOS amplifiers cascode design such as high quiescent power consumption, poor power utilization in common-source stage cascodes and poor large-signal slew-rate performance.

A low power CMOS operation amplifier using gm/ID Methodology with 68dB DC gain, 30 MHz bandwidth, phase margin of 58 with a power dissipation of only 63 W has been presented.

Keywords - CMOS, Low-Power, Operational Amplifier, gm/ID Methodology

I. INTRODUCTION

The growing adoption of portable electronics devices, the increasing use of the wearable device in healthcare solutions, implanted medical devices and the growing development of Internet of Thing devices sensor nodes, have changed entirely the IC design methodology. In fact, such device needs to operate throughout all the operation life with only one battery device, even during month and years, going down from coin-cell sizes up to thin-film micro batteries. Any little amount of consumed energy may be the factor in which determine the costs, weight and the size of devices and moreover its portability and, indeed two-stage op-amp, in the analog field constitutes one the key building block commonly deployed for the solution of wide array problems both in Voltage Follower and ADCs, Filters.

1.1 Motivation behind low-Power Analog Circuits:

Portable / wearable electronics: the percentage adoption on wearable electronic (ex: Health bands, watches, patches) increase exponentially every year. Nowadays these systems run with small coin, long-lasting and thin-film micro battery. Therefore analog front-end circuits in these devices must keep high signal integrity in order to minimize power consumption. Biomedical systems: this category includes cochlear implants, pacemakers, neural recorders and pharmaceutical delivery systems. Because of the fact that batteries must be placed inside the organism and thus the possibility to change the mis-related to the surge.

Internet of Thing and Wireless sensor nodes IoT sensors are usually placed in the positions where access to the electrical energy is problematic (eg. Remote colonies). For this reason, energy scavengers or long time lasting batteries are adopted. Then analog interfaces circuit must be efficient in order to guarantee a long lifetime.

II. LITERATURE REVIEW

The design of CMOS based op-amps has been initiated by a number of engineers. Works of Gray and Meyer were presumably the earliest as they emphasized parameters necessary for basic reliable operation in an opamp, a stable operation and relatively high voltage gain. Allen and Holberg made the next significant step in the development of CMOS op amp dynamics by devising systematic design techniques based on load transistor sizing and compensation to guarantee stability.

A good addition to developing this field was Baker in 2008, who will present design techniques that facilitate making CMOS op amp more efficient, using current mirrors and differential input stage to save on power.

Razavi's contribution to this field was concerned on the limits of downscaling and latest developments in reducing supply voltage present developing difficulties in.

Preamplifiers are among one of the earliest circuit uses of high gain, high speed components. Though traditional OP-amps were built to operate fast and with high gain, they often needed high supply voltage and packed quite a lot of power while operating. Minimizing power consumption without degrading typical performance specifications such as gain, bandwidth, input characteristics, and stability remains an active area of research.

III. PROPOSED METHODOLOGY AND SYSTEM DESIGN

3.1 System Design Specifications

The low-power two stage CMOS operational amplifier proposed is designed with 180nm process technology. The main motivation for designing this op-amp topology is to achieve an op-amp structure that is suitable for power-constrained biomedical instrumentation systems and other portable biomedical devices. The design must achieve the following specifications, power requirement: open-loop voltage gain ≥ 60 dB (1000 V/V) to get less gain error and nonlinearities; unity-gain bandwidth ≥ 30 MHz to process audio-band and biomedical-band signals; phase margin ≥ 55 to ensure in-amp stability; power requirement: power consumption must be less than 150 W.

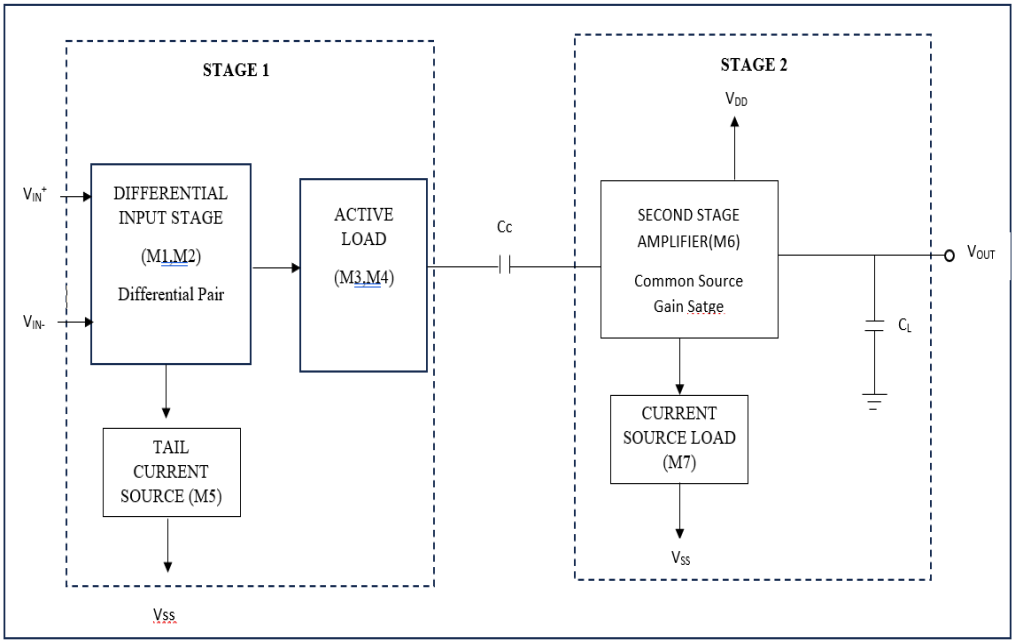

fig.1.proposed 7-transistor cmos op-amp architecture

3.2 Topology Selection

Two-stage CMOS architecture has been used for the following reason: it effectively separates the amplification of the input signal within the first stage from the driving of the output voltage within the second stage in order to optimize them separately. Single stage topology which provide high gain (e.g. Telescopic or folded cascodes) suffer in the minimum voltage and low-power regime due to cascode transistors stacking reducing the available output swing. The first stage of amplification uses an NMOS differential input pair biased from the negative supply rail, a combination which fits termperas-are-optimized well with a PMOS current mirror as an active load.

IV. IMPLEMENTATION

The implementation was coded at the transistor level, using 180nm CMOS technology with 1.8V supply voltage; it has been simulated using Cadence Virtuoso/LTSpice.

4.1 First-Stage and Biasing Implementation

The beginning of the circuit (the input stage) contains an NMOS differential pair (M1, M2) biased by a PMOS current mirror (M3, M4), subjected to a bias by the tail current generator (M5). During the operation, transistors have the same drain current of 9.533 A with a transconductance of 181.6 S, giving a gm/ID of the order of 19 S/A. The circuit exhibits the best low power behavior due to its working point in the moderate-weak inversion region. The output resistance of the first stage is about 374 k, with an input first stage voltage gain of 67.9 V/V (36.6 db).

4.2 Second-Stage and Compensation

The second common-source gain stage is using a PMOS (M6) and NMOS (M7) transistor, which provides a further voltage gain of (3.53 V/V (11 dB)). Reference currents are still provided by biasing network of M0 and M8 transistor. To enable frequency domain stability, Miller compensation is introduced with 1 pF capacitor (Cc) and a nulling resistor. The overall amplifier quiescent current is approximately 35 A, which is about 63 W of power.

V. RESULTS AND DISCUSSION

In the first-cut design, the DC gain was ~65 dB, phase margin was >60, but UGB, was only ~18MHz at VIP=0.8V. To find the optimum between bandwidth, the power and phase margin design goals, the following optimization was made:

- **Iteration 1:** Increasing the width (W1) of the input transistors raised the UGB to 25 MHz, but lowered the phase margin to 55°.

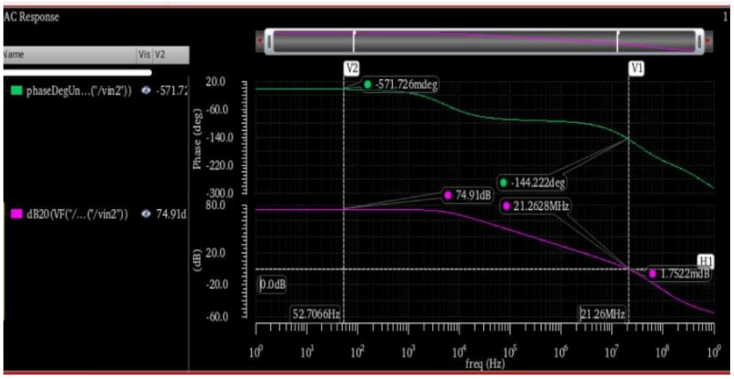

Figure 5.1: AC response after increasing the width (W1) of input transistors M1 and M2.

- **Iteration 2:** Raising the bias current (Iref) to 24 µA successfully improved the UGB to 45 MHz, but significantly degraded the phase margin to 45° and increased power consumption to 86 µW.

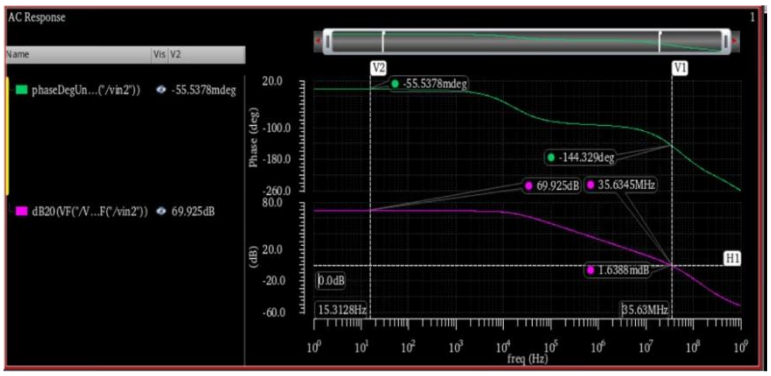

Figure 5.2: AC response after increasing the bias current Iref to 24 µA.

- **Iteration 3:** Reducing the channel length of the M6 transistor from 1 µm to 0.5 µm successfully reduced parasitic capacitance at the critical node (CDD) by approximately 50%, restoring the phase margin back to 55°.

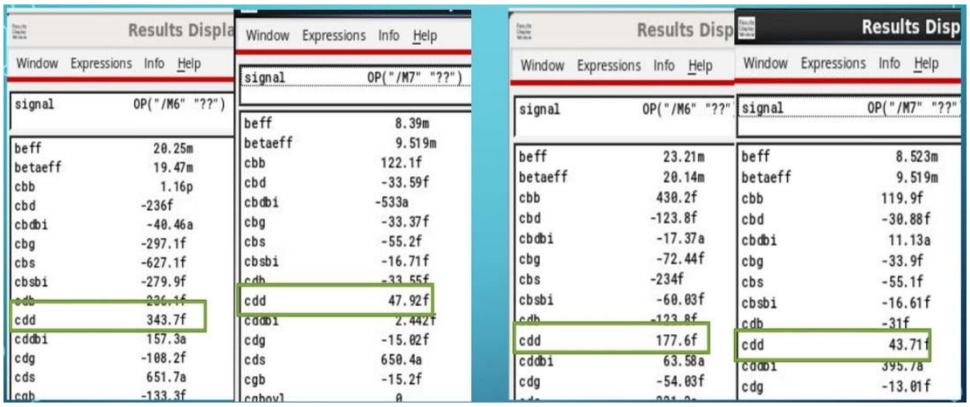

Figure 5.3: Reduction in parasitic capacitance (CDD) at the critical node when the channel length of transistor M6 is reduced from 1 µm to 0.5 µm.

- **Final Optimization:** To lower power consumption while keeping the UGB exactly at 30 MHz, Iref was reduced from 24 µA to 14 µA.

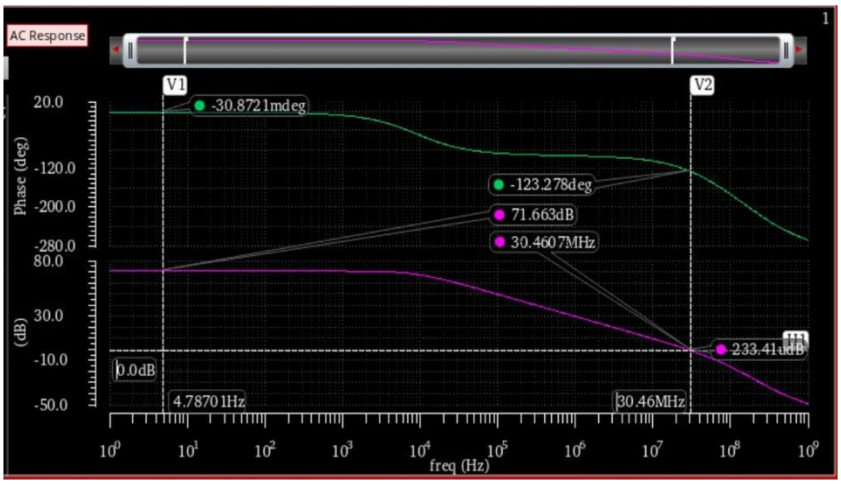

Figure 5.4: Final optimized AC response after reducing Iref from 24 µA to 14 µA

table 1: final performance vs. target

Parameter	**Target**	**Achieved**
DC Gain	≥ 60 dB	68 dB
UGB	≥ 30 MHz	30 MHz
Phase Margin	≥ 55°	58°
Power	≤ 150 µW	63 µW
ICMR	0.6 - 1.2 V	0.6 - 1.3 V
Output Swing	≥ 1.2 Vpp	1.4 Vpp
Slew Rate	≥ 5 V/µs	8 V/µs

VI. CONCLUSION AND FUTURE SCOPE

This paper presented an optimized low power 2-stage CMOS OC amplifier was fabricated and 1.8V power supply by gm/ID approach. With the iterative design and optimization approach was ultimately achieved a DC gain=68dB, BW=30MHz, phase margin=58, and power dissipation=63W, input common-mode voltage is [0.6 V, 1.3 V], output swing=1.4 Vpp, Slew rate=8 V/ s, the other parameters obtained. This based on tht op-amp can be used for low power design applications such as body ECG/EEG sensors, wireless sensor nodes, and other IoT applications.

Further operational improvement may also be achieved by modifying the output stage to a class-AB stage which would allow for a increased slew rate and settling time with minimal quiescent power consumption. The use of a complementary PMOS differential pair could also achieve a rail-to-rail input common mode voltage range with the substitution of a dynamic adaptive biasing element. This would allow for a power saving condition during quiescent conditions.

REFERENCES

[1] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed. Hoboken, NJ, USA: Wiley, 2009.
[2] B. Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed. New York, NY, USA: McGraw-Hill, 2016.
[3] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd ed. New York, NY, USA: Oxford University Press, 2002.
[4] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, 3rd ed. Hoboken, NJ, USA: Wiley, 2010. [5] F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," IEEE Journal of Solid-State Circuits, vol. 31, no. 9, pp. 1314-1319, Sep. 1996.