DESIGN OF APPROXIMATE ADDER WITH RECONFIGURABLE ACCURACY

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Abstract : Approximate computing is a useful method of making faster and more energy efficient approximation circuits for arithmetic circuits useful in an error-tolerant application. The paper proposes an approximate adder with reconfigurable accuracy based on the segmentation technique using ternary logic. The proposed 6-trit adder splits the computation into several segments to minimise the propagation delay of the carries and allow parallel processing. The approximation of the modules is done in the lower segments, and the exact calculation is kept in the most significant segment. A 3-stage reconfiguration mechanism, HA1, HA2 and TOR blocks, gradually enhances the output accuracy. Clock gating is used to eliminate the unnecessary switching activity and dynamic power consumption. The design is synthesized and verified using Verilog HDL and Xilinx Vivado by simulation, synthesis, timing, power and resource analysis. The accuracy of approximation is evaluated using Normalized Error Distance (NED) and the practical performance is evaluated by applying an image blending application. The results demonstrate that the proposed architecture is effective in terms of speed, power consumption, and computational accuracy.
Keywords— Approximate Computing, Ternary Adder, Reconfigurable Accuracy, Segmentation, Clock Gating, NED.

I. INTRODUCTION

Arithmetic circuits for modern digital systems must be fast, consume as little power as possible, and use as little hardware as possible. Adders are extensively used for processor applications, signal processing, multimedia and image processing. However, conventional exact adders have long carry propagation paths and are typically slow and consume more power. To solve this problem, approximate computing allows for intentional errors in the computations to enhance performance metrics, including speed, area, and power. Approximate Arithmetic Circuits have received much attention as many Multimedia and Image Processing applications are at least as tolerant of small errors. In this paper, an approximate ternary adder reconfigurable in accuracy based on segmentation is proposed. The architecture minimizes carry propagation delay by breaking up the computation in a segmented way and takes advantage of multiple reconfiguration stages to gradually enhance accuracy. There is also clock gating to minimize dynamic power consumption.

II. LITERATURE SURVEY

Vendhan et al. [1] introduced an approximate ternary adder with reconfigurable accuracy based on segmentation, which helped to reduce the propagation delay of the carry and increase the power-delay product for image processing applications. A ternary full adder with lower power consumption and higher energy efficiency was designed by Hashemipour et al. [2] using 21 CNTFETs. The approximate arithmetic architecture proposed by Lee et al. [3] was optimized for the area, power and accuracy tradeoff by configuration super sampling in FPGA. In order to enhance the energy efficiency, Chen et al. [4] proposed a reconfigurable approximate/accurate processor architecture that dynamically changed the accuracy of the computations. Malik et al. [5] presented an approximately CNTFET based ternary full adder which reduced hardware complexity and power consumption for the use in multimedia applications. Malik et al. [6] also examined the power benefits of approximate designs of ternary full adders in comparison to exact designs based on CNTFETs. To reduce the hardware complexity and energy consumption, Bastani et al. [7] proposed an energy and area efficient approximate ternary adder based on CNTFET switching logic. Mukaidono [8] laid the theoretical groundwork of ternary logic using regular ternary logic functions and they are still used to develop new ternary arithmetic systems. These studies show that while there has been a significant effort to enhance the power efficiency and computational speed of power systems, little research has been conducted on segmentation-based ternary adders that have reconfigurable accuracy and power optimisation.

III. RESEARCH METHODOLOGY

This proposed work is based on the 6-trit segmentation based approximate adder with reconfigurable accuracy based on ternary logic. In the present design, the architecture splits the whole adder into three independent segments to minimize carry propagation delay and to perform the computation in parallel as shown in Fig 1. The lower-order digits are used to perform approximate arithmetic, while the most significant digit is used to perform correct arithmetic to ensure output quality.

A. Segmentation Technique

The proposed architecture is a segmentation technique proposed in fig 1 which divides the 6-trit adder into 3 independent segments. The most important segment has accurate computation using FA1 and HA blocks and the lower segments use approximate computation with HA blocks. This eliminates the propagation of the carry from one of the lower segments into the others, allowing multiple operations to be performed simultaneously, which decreases the critical path delay and speeds up the calculation. This also simplifies hardware and improves the overall performance.

B. Reconfigurable Accuracy

In order to enhance the output accuracy, a three-stage reconfiguration mechanism is added to the proposed architecture as depicted in Fig (1). In the approximate mode, the adder is used to provide high speed approximate computation at the cost of minimal hardware. During the approximation phase, HAC and HA1 blocks generate and use intermediate carry details which were ignored during the approximation phase. In Stage 3, further HA1 and TOR blocks are switched-on to further correct the output and to compute almost exactly. This reconfiguration process allows the architecture to dynamically balance computational accuracy and hardware efficiency according to application requirements.

C. NED Evaluation

Normalized Error Distance (NED) is used to assess the accuracy of the proposed approximate adder. The difference between actual output and estimated output (compared to the maximum possible output value is measured by NED). The lower the NED, the more accurate the calculations; the higher the NED, the more of an error approximation. To ensure the effectiveness of the proposed mechanism for improving accuracy, NED analysis is carried out at different reconfiguration stages.

$ED = Vexact - Vapprox$ (3.1)

$NED = Vexact - Vapprox / Vmax$ (3.2)

where V(exact) is the exact output value, V(approx.) is the approximate output value, and V(max) is the maximum possible output value.

D. Clock Gating and Image Blending Application

The proposed design includes clock gating to minimize power consumption and switching activity. The glitch-free operation and disabling of unused sections of the circuit is accomplished using a latch-based clock gating structure. The proposed adder is then tested using an image blending application for further validation of the effectiveness. The images are blended using the approximate adder and the quality of the output image is assessed by Peak Signal-to-Noise Ratio (PSNR) in grayscale. The results obtained in this work show that the proposed architecture has high image quality, a better power efficiency and computational performance.

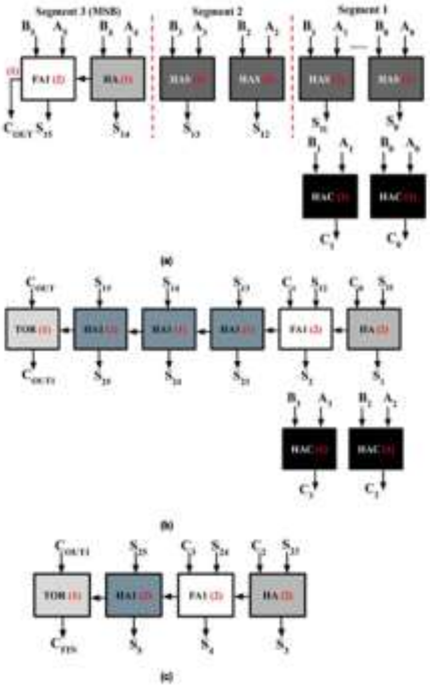


fig. 1. proposed 6-trit reconfigurable approximate adder architecture

IV. RESULTS AND DISCUSSION

A. Functional Verification

The simulation wave form checks the correct working of the proposed segmentation based approximate adder. Various ternary input combinations were used, and the output of both the stage 1, stage 2, stage 3 and exact adder were noted. This can be observed as the accuracy gets increasingly better as the reconfiguration stages go. The output of the final stage 3 is very close to the exact output of the adder, showing the effectiveness of the reconfigurable accuracy mechanism.

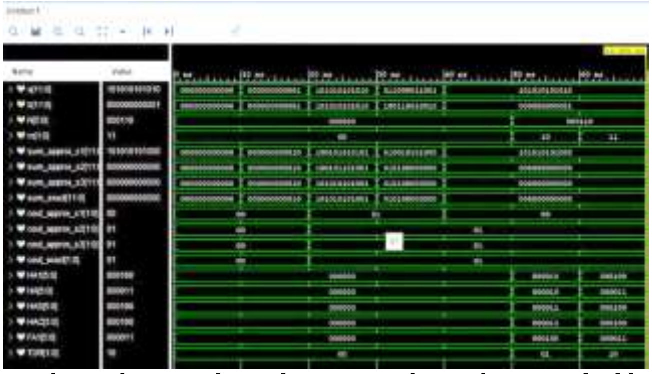


fig. 2. functional simulation waveform of proposed adder

B. NED Analysis

The NED simulation waveform presents the error analysis done on the proposed architecture. The Error Distance (ED) and NED values are obtained by comparing the approximate outputs to the exact outputs. Additional correction circuits result in a decrease in error from Stage 1 to Stage 3. The last step reaches zero error, which means that the reconfiguration process also corrects the exact computation when needed for higher accuracy.

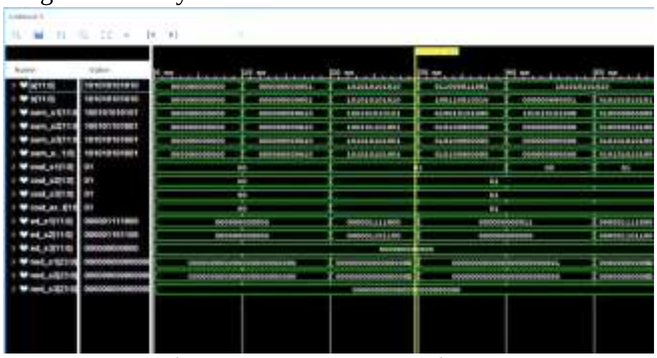


fig. 3. ned analysis waveform

The effect of the reconfiguration stages on the computational accuracy is presented in the NED and ED analysis results listed in Table I. If the lack of carry correction is the reason, then the error in the output in stage 1 is the largest since there is no carry correction. In Stage 2, the error is minimized by using the HAC and HA1 blocks. Finally, the error is completely removed in Stage 3, giving an NED value of zero and an output of the exact adder.

table i: ed and ned results

Stage	ED	NED
Stage 1	120	54
Stage 2	108	49
Stage 3	0	0

C. Clock Gating Analysis

The clock gating waveform is used to validate the power optimization technique used in the proposed design. If the enable signal is active, the gated clock will be the same as the original clock and the circuit will function normally. If the enable signal is set to low, the gated clock is set to low, which means that there will be no unnecessary switching activity. This verifies correct functionality of the latch based clock gating structure and its ability to reduce dynamic power consumption.

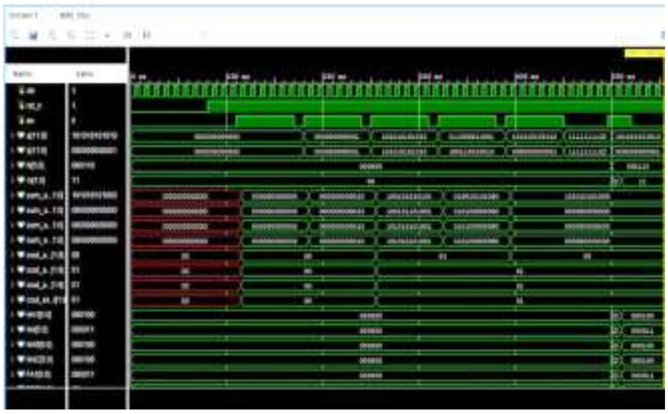


fig. 4. clock gating simulation waveform

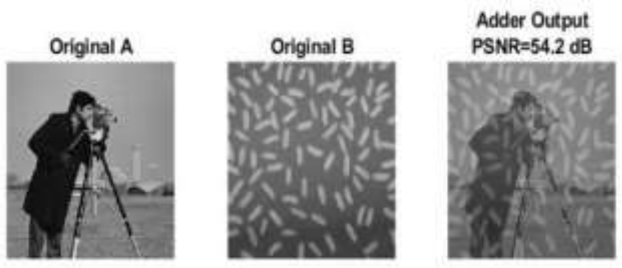
The above clock gating results prove the effectiveness of the proposed technique of power optimisations. As a result of masking the unnecessary switching activity during an inactive period, there is a substantial reduction in dynamic power consumption. It is implemented while preserving the correct functionality of the circuit, in a much lower power consumption. These results validate the overall energy efficiency of the proposed architecture achieved by clock gating, while maintaining performance.

table ii: clock gating results

Parameter	Without Clock Gating	With Clock Gating
Total Power (W)	10.01	0.132
Dynamic Power (W)	9.838	0.002

D. Image Blending Validation

An image blending application was used as a test to see if the proposed architecture was practical. Two grayscale images were added together approximately and the output was tested with Peak Signal-to-Noise Ratio (PSNR). The PSNR value of 44.2 dB obtained shows that the blended image has very less distortion and maintained the high quality of the image. The result proves the



proposed architecture suitable for the error tolerant image processing application.

Fig. 5. Image Blending Output

E. Performance Comparison of Proposed Architecture

table iii: performance analysis

Parameter	Exact Adder	Approximate Adder	Clock-Gated Exact Adder	Clock-Gated Approximate Adder
Total Power (W)	10.01	9.838	0.132	0.132
Dynamic Power (W)	9.838	9.667	0.002	0.002
Static Power (W)	0.172	0.171	0.131	0.131
Slice LUTs	23	43	24	36
Slice Registers	-	-	15	15
Bonded IOBs	38	38	41	41
Maximum Delay (ns)	7.024	7.808	2.328	2.328
Error Distance (ED)	0	120-> 108-> 0	0	0
NED Value	0	54-> 49-> 0	0	0
PSNR (dB)	-	54.2	-	54.2
Accuracy	Exact	Reconfigurable Accuracy	Exact	Reconfigurable Accuracy + Power Optimization

The Table III demonstrates that the proposed architecture is able to balance accuracy of computation and hardware efficiency. The approximate design minimizes power usage and provides progressive accuracy improvement (reconfiguration). Moreover, clock gating significantly reduces the dynamic power consumption. As a result of blending the images and the NED analysis, the proposed architecture is found to be appropriate for the low power and error-tolerant applications.

V. CONCLUSION

This paper proposed an approximate adder reconfigurable accuracy based on paper segmentation method with ternary logic. The proposed architecture mitigates the carry propagation delay by breaking up the computation in segments and enhances accuracy with the help of a three-stage reconfiguration. The progressive error reduction was verified by NED analysis and dynamic power consumption was reduced by clock gating. The PSNR of the image blending application was 54.2 dB, which proves the feasibility of the design in error-tolerant applications. The results achieved show that the proposed architecture can be an effective solution in terms of computational accuracy, power efficiency and hardware performance.

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