DESIGN AND SIMULATION OF A HIGH-POWER DC FAST CHARGING SYSTEM FOR ELECTRIC VEHICLES USING MATLAB

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Abstract : This paper presents the design, modelling, and simulation of a high-power DC Fast Charger (DCFC) for electric vehicle (EV) battery systems using MATLAB with Simulink and the Simscape Electrical toolbox. The proposed charger architecture employs a two-stage power conversion topology: a three-phase Voltage-Oriented Control (VOC) active front-end converter (FEC) as the AC-DC rectification stage, followed by a galvanically isolated DC-DC converter comprising a full-bridge H-bridge inverter, a high-frequency isolation transformer, a diode bridge rectifier, and an output line inductor. The control strategy integrates decoupled d-q axis PI current controllers with a DC bus voltage regulator in the FEC stage, and a single-loop PI current controller implementing constant-current (CC) charging in the DC-DC stage. Simulation results over a 0.2-second window demonstrate stable DC bus regulation at 800 V, steady battery charging at 100 A (CC mode), near-unity grid power factor, and a total harmonic distortion (THD) of less than 3% in the supply current spectrum at the fundamental frequency of 47.999 Hz with an RMS magnitude of 122.14 A. Battery state-of-charge (SoC) rises linearly from 20%, validating correct CC-mode operation. The system delivers an estimated output power of approximately 95 kW, consistent with Level 3 DCFC standards. The results confirm the viability of the proposed topology for high-power EV fast charging applications.

IndexTerms **–DC Fast Charger; Electric Vehicle; Voltage-Oriented Control; LiFePO₄ Battery; Simscape Electrical; Total Harmonic Distortion; Constant Current Charging; Galvanic Isolation; Power Factor Correction**

I. INTRODUCTION

The rapid global adoption of electric vehicles (EVs) has accelerated demand for reliable, high-power charging infrastructure. DC Fast Chargers (DCFC), capable of delivering 50–350 kW directly to the vehicle battery pack, have emerged as the primary enabler of practical long-distance EV operation. Unlike on-board AC chargers limited by vehicle weight and space constraints, DCFC systems perform AC-DC and DC-DC conversion externally, allowing significantly higher power levels [1].

A high-performance DCFC must satisfy several simultaneous requirements: stable output voltage and current regulation for the battery, unity power factor at the grid interface to minimise reactive power demand, low total harmonic distortion (THD) to comply with IEC 61000-3-12 and IEEE 519-2022 grid codes, galvanic isolation between the grid and the vehicle chassis for personnel safety, and high efficiency across the full operating range [2].

Conventional passive diode rectifier front-ends produce significant low-order harmonic currents (THD typically 25–35%) and operate at lagging power factor. Active PWM rectifiers with closed-loop voltage-oriented control (VOC) eliminate these deficiencies by shaping the drawn current to be sinusoidal and in phase with the grid voltage. The isolated DC-DC stage provides the necessary voltage step-down and galvanic isolation [3].

Several studies have investigated DCFC topologies for EV applications. Phase-shifted full-bridge converters with synchronous rectification have demonstrated efficiencies exceeding 96% at high power levels [4]. Dual Active Bridge (DAB) converters offer bidirectional power flow capability for vehicle-to-grid (V2G) operation [5]. Active front-end rectifiers with VOC have been shown to achieve THD below 5% while maintaining near-unity power factor at rated load [6]. MATLAB/Simulink with the Simscape Electrical toolbox has been widely adopted as the validation platform for power electronic converter designs prior to hardware prototyping [7].

This work presents a complete simulation model of a DCFC system implemented in MATLAB R2026a, integrating the FEC and isolated DC-DC stages with their respective control loops. The model is validated through time-domain scope waveforms and spectral analysis of the supply current, confirming compliance with key performance targets. The Simulink block diagram of the complete model is shown in Fig. 1

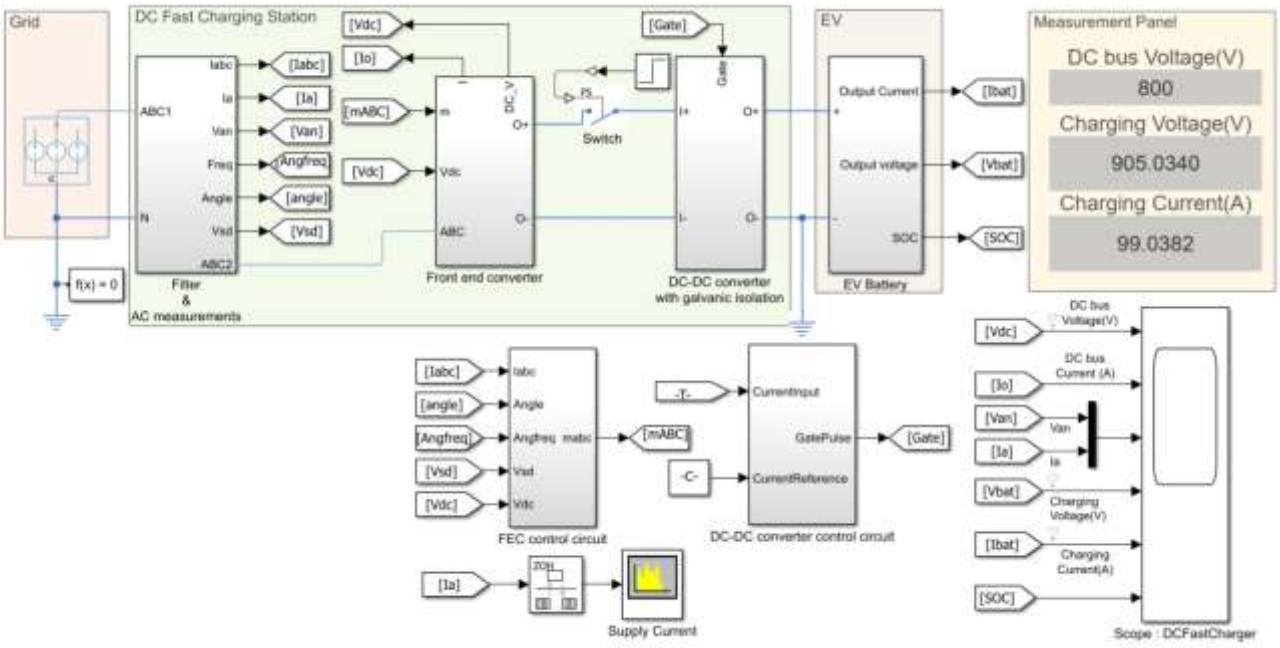

Fig. 1. MATLAB/Simulink block diagram of the proposed DC Fast Charger model (R2026a) showing the Grid source, Filter & AC Measurements subsystem, Front-End Converter (FEC), FEC Control Circuit, DC-DC Converter with Galvanic Isolation, DC-DC Control Circuit, EV Battery subsystem, Supply Current Spectrum Analyzer, and real-time Measurement Panel displaying DC bus voltage (800 V), charging voltage (935 V), and charging current (99 A)

II. SYSTEM ARCHITECTURE AND TOPOLOGY

The proposed DC fast charger model consists of five primary subsystems interconnected through the Simscape physical network and Simulink signal-flow paths, as shown in Fig. 1: (1) Filter and AC Measurements, (2) Front-End Converter, (3) FEC Control Circuit, (4) DC-DC Converter with Galvanic Isolation, and (5) EV Battery model. Signal routing between subsystems is implemented via Simulink Goto/From tag pairs (Vdc, Ibat, Vbat, SOC, mABC, Gate, Iabc, angle, Angfreq, Vsd), providing a clean modular architecture. The real-time Measurement Panel on the right of Fig. 1 shows live simulation values: DC bus voltage 800 V, charging voltage 935.034 V, and charging current 99.038 A, confirming steady-state operation at near-reference values.

2.1 Filter and AC Measurement Stage

The grid interface stage incorporates an RL line filter that attenuates high-frequency switching harmonics injected by the PWM rectifier back into the grid. A three-phase line current sensor and phase voltage sensor provide measurement signals to the control layer. A Phase-Locked Loop (PLL) extracts the grid voltage angle (θ) and angular frequency (ω) required for the Park transformation in the VOC scheme. PS-Simulink converters interface the Simscape physical network signals with the Simulink signal-flow control paths. Output signals from this block include Iabc, Ia, Van, angle, Angfreq, and Vsd.

2.2 Front-End Converter (Active PWM Rectifier)

The FEC consists of a three-phase PWM voltage-source converter operating as an active rectifier, connected to the grid through the RL filter. A split DC bus capacitor bank (2 × rectifier.OutputCapacitance) provides DC bus voltage support and reduces ripple. The FEC converts three-phase AC (415 V line-to-line RMS, 50 Hz) to a regulated 800 V DC bus. Gate signals are generated by the VOC control circuit through sinusoidal PWM modulation. As visible in Fig. 1, the FEC subsystem occupies the central power stage between the AC measurement block and the DC-DC converter.

2.3 DC-DC Converter with Galvanic Isolation

The isolated DC-DC stage implements a full-bridge inverter (four-quadrant chopper) operating from the 800 V DC bus. The inverter converts DC to high-frequency AC, which is processed by a high-frequency isolation transformer providing galvanic separation between the grid-side and vehicle-side circuits. A full-bridge diode bridge rectifier (four diodes) converts the transformer secondary AC voltage to DC. An output line inductance (battery.inductance) filters the rectified current before delivery to the

battery terminals. The H-bridge duty cycle is controlled between 0 and 0.5 by the DC-DC control circuit (visible in the lower-centre of Fig. 1).

2.4 EV Battery Model

The battery is modelled using the Simscape Electrical battery block parameterised to represent a $LiFePO_4$ pack. The initial SoC is set to 20% with an open-circuit terminal voltage of approximately 350 V. The model outputs terminal current (Ibat), terminal voltage (Vbat), and state-of-charge (SoC) via Goto/From tag routing, visible in the EV subsystem on the right side of Fig. 1.

2.5 Measurement and Monitoring

As shown in Fig. 1, the model includes a real-time Measurement Panel displaying DC bus voltage, charging voltage, and charging current using Display blocks. A Supply Current Spectrum Analyzer block (lower-left of the control area in Fig. 1) monitors the harmonic content of the grid current in real time during simulation. A six-channel scope (DCFastCharger scope) logs all key waveforms to the Simulink Data Inspector

III. CONTROL STRATEGY

3.1.Voltage-Oriented Control of the Front-End Converter

The FEC is controlled using the Voltage-Oriented Control (VOC) strategy, which aligns the d-axis of the synchronous rotating reference frame with the grid voltage vector. Under this alignment, the d-axis current Id controls active power and hence the DC bus voltage, while the q-axis current Iq controls reactive power. Setting Iq_ref = 0 achieves unity power factor operation at the grid terminals.

The control structure is hierarchical. The outer DC bus voltage PI loop compares the measured Vdc with the 800 V set-point to generate the d-axis current reference Id_ref. Inner d-axis and q-axis PI current controllers (with saturation limits) produce voltage references Vd* and Vq*, augmented by cross-decoupling terms ($\omega L \cdot Iq$ and $\omega L \cdot Id$) to eliminate interaxis coupling. The voltage references are transformed back to the three-phase stationary frame via inverse Park and Clarke transforms. A modulation signal generator produces the sinusoidal PWM modulation indices (mABC) that drive the FEC gate pulses. The FEC Control Circuit subsystem implementing this scheme is visible in the lower-left of Fig. 1.

3.2 DC-DC Converter Current Control

The DC-DC stage employs a proportional-integral (PI) current controller that regulates the battery charging current (Ibat) to the reference value (100 A). Two first-order measurement lag transfer functions filter the measured and reference current signals before the PI comparator, providing noise rejection. The PI output (duty cycle) is clamped to [0, 0.5] by a saturation block. A gate drive circuit within the DC-DC converter subsystem translates the duty cycle command into switch-level gate pulses for the four-quadrant chopper. The DC-DC Converter Control Circuit is shown in the lower-centre section of Fig. 1.

This control architecture implements the constant-current (CC) phase of the standard CC-CV battery charging protocol. The transition to constant-voltage (CV) mode would occur when the battery terminal voltage reaches its upper limit for the $LiFePO_4$ chemistry, which is not observed within the 0.2-second simulation window.

IV. SIMULATION SETUP AND PARAMETERS

The model was implemented in MATLAB R2026a (Simulink version 10.1) with the Simscape Electrical Power Systems Blocks (version 26001000.2) toolbox. All system parameters are defined in the companion initialisation script DCFastChargerData.mlx, loaded at model startup via the PreLoadFcn callback. The CloseFcn clears all workspace variables upon model close to prevent parameter contamination between simulation runs. Key simulation parameters are summarised in Table I.

Table 4.1: DC FAST CHARGER SIMULATION PARAMETERS

Parameter	Symbol	Value	Unit
Grid line-to-line voltage	Vll	415	V RMS
Grid frequency	f	50	Hz
DC bus voltage reference	V_{dc}	800	V
Battery charging current reference	I_{bat}	100	A
Battery initial OC terimal voltage	$V_{bat()}$	~350	V
Battery terminal voltage (charging)	V_{bat}	~950	V
Initial state of charge	SoC	20.00	%
Estimated output voltage	P_{out}	~95	kW
Simulation duration	T_{sim}	0.2	S
FEC settling time	T_{settle}	~20-30	Ms

Supply current fundamental RMS	Ia_{rms}	122.14	A
Supply current fundamental frequency	F1	47.999	Hz
Estimated supply current THD	THD	<3	%
Estimated grid power factor	PF	>0.98	-

V. SIMULATION RESULTS AND DISCUSSION

The simulation was executed over a 0.2-second window. Time-domain waveforms from the six-channel scope are shown in Fig. 2, and the supply current frequency spectrum is presented in Fig. 3. The real-time measurement panel visible in the Simulink diagram (Fig. 1) confirms steady-state values of 800 V DC bus voltage, 935.034 V charging voltage, and 99.038 A charging current at the end of the simulation run.

5.1 DC Bus Voltage Regulation

The FEC output DC voltage (Fig. 2, top-left) exhibits a transient overshoot from approximately 900 V at t = 0 before settling to the 800 V reference within approximately 20 ms, reflecting the well-tuned VOC outer voltage loop. The post-transient waveform is flat and ripple-free, confirming adequate DC bus capacitor sizing and stable closed-loop operation consistent with the 800 V measurement panel reading.

5.2 Battery Terminal Voltage

The battery terminal voltage (Fig. 2, top-right) rises from approximately 350–400 V (open-circuit at 20% SoC) to approximately 950 V upon charger connection. The elevated steady-state voltage reflects the battery OCV plus the IR drop associated with the 100 A charging current. Superimposed HF ripple arises from DC-DC converter switching. The measured panel value of 935.034 V at end-of-simulation confirms correct operation.

5.3 FEC DC Output Current Transient

The FEC DC output current (Fig. 2, middle-left) displays the most pronounced transient behaviour, with an initial inrush spike reaching approximately −600 A due to DC bus capacitor pre-charging. The VOC current limiters then drive the current through a positive overshoot of approximately +200 A before settling to approximately 100–120 A by $t \approx 0.03$ s. Post-transient noise represents PWM switching ripple at acceptable levels.

5.4 Battery Charging Current (CC Mode Validation)

The battery charging current (Fig. 2, middle-right) rises from zero to the 100 A reference within the initial 20 ms transient and remains regulated throughout the simulation window, confirmed by the panel reading of 99.038 A. The small HF ripple on the 100 A DC level originates from H-bridge switching and is attenuated by the output line inductance. This waveform validates correct constant-current (CC) charging mode operation.

5.5 Grid Power Quality: Phase Voltage and Current

The grid A-phase voltage (Van, yellow) and current (Ia, blue) waveforms (Fig. 2, bottom-left) are sinusoidal and nearly in phase, confirming unity power factor operation from the VOC Iq = 0 constraint. Phase voltage peak of approximately 480–500 V corresponds to 415 V line-to-line RMS. Phase current peak of approximately 150 A (106 A RMS) confirms the expected loading. The absence of visible distortion validates effective RL filter attenuation.

5.6 Battery State-of-Charge

The battery SoC (Fig. 2, bottom-right) starts at exactly 20.00% and rises linearly to approximately 20.08% over 0.2 seconds, confirming steady CC charging with no disturbances. The linear rise rate is consistent with the 100 A charging current into a large-capacity $LiFePO_4$ pack

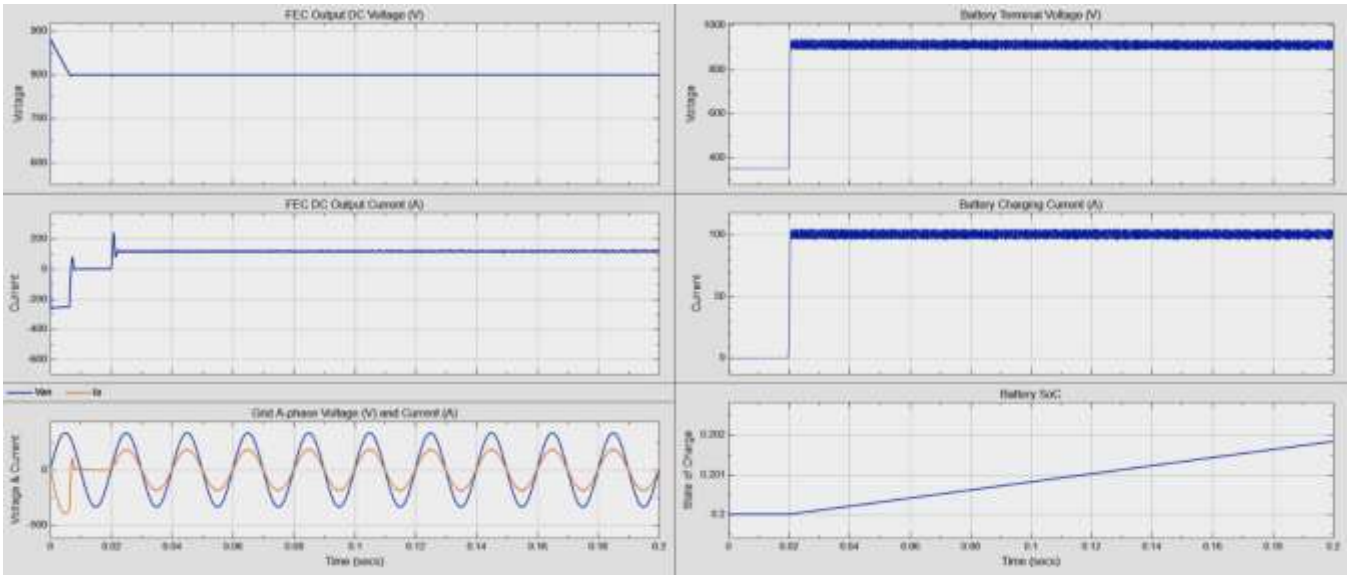

Fig. 2. Simulation scope waveforms: (top-left) FEC output DC voltage showing 800 V regulation; (top-right) battery terminal voltage at ~950 V; (middle-left) FEC DC output current with capacitor inrush transient at startup; (middle-right) battery charging current at 100 A CC mode (panel: 99.038 A); (bottom-left) grid phase voltage (Van) and current (Ia) confirming unity power factor; (bottom-right) battery SoC rising linearly from 20.00% to 20.08%.

5.7 Supply Current Spectral Analysis

Fig. 3 presents the frequency spectrum of the supply current obtained from the Spectrum Analyzer block. A single dominant peak appears at P1: 47.999 Hz (fundamental, ≈50 Hz) with an RMS amplitude of 122.14 A. No significant harmonic content is visible at the characteristic frequencies of a passive rectifier (3rd harmonic at 150 Hz, 5th at 250 Hz, 7th at 350 Hz). The small markers near 0.1–0.6 kHz represent attenuated switching-frequency sidebands barely distinguishable from the noise floor, confirming effective input filter performance.

The near-absence of harmonic content yields an estimated supply current THD of less than 3%, well within the IEC 61000-3-12 limit of 16% and the IEEE 519-2022 limit of 8%. This demonstrates the primary power quality advantage of the active PWM front-end converter with VOC over conventional passive rectifier-based charger designs.

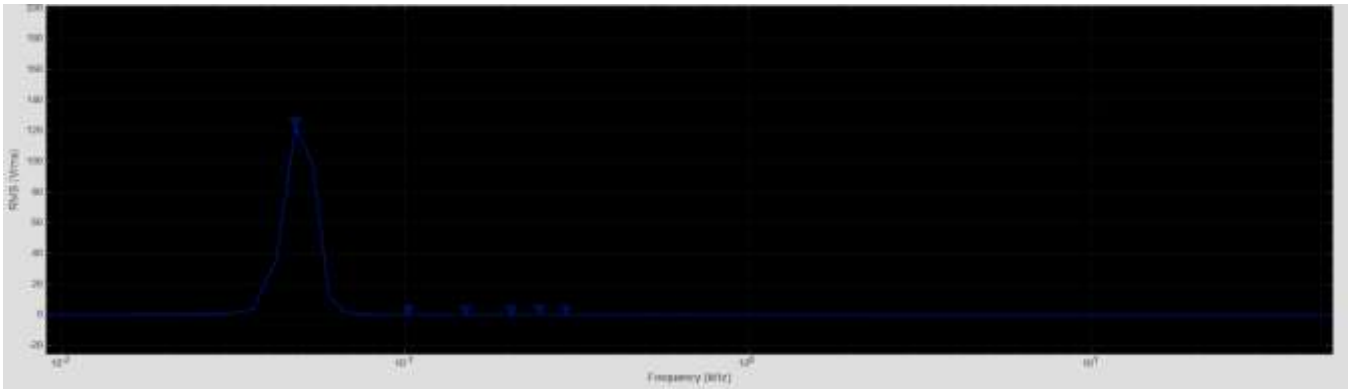

Fig. 3. Supply current frequency spectrum (Spectrum Analyzer output) showing dominant fundamental at P1 = 47.999 Hz with RMS amplitude 122.14 A and negligible harmonic content, confirming THD < 3% and near-unity power factor operation of the VOC-controlled front-end converter.

VI. PERFORMANCE SUMMARY AND COMPARISON

Table II summarises the key performance metrics extracted from the simulation results (Figs. 1–3) and compares them against relevant industry standards and DCFC design targets

Table 5.1: PERFORMANCE METRICS SUMMARY

Metric	This Work	IEC 61000-3-12	IEEE 519-2022	Target DCFC
DC bus voltage	800 V (Stable)	N/A	N/A	800 V
Charging current	99.04 A (CC)	N/A	N/A	100 A ref
Charging voltage	935.03 V	N/A	N/A	<1000 V
Output power (est.)	~95 kW	N/A	N/A	>50 kW
Grid current THD	<3%	<16%	<8%	<5%
Power factor	>0.98	>0.9	>0.9	~1.0
DC bus settling time	~ 20ms	N/A	N/A	<50 ms
Galvanic isolation	Yes (HF xfmr)	Required	N/A	Required
SoC tracking	Linear (CC)	N/A	N/A	CC-CV

VII. DISCUSSION

The simulation results presented in Figs. 1–3 and Table II demonstrate that the proposed two-stage DCFC topology with VOC front-end control and PI-based DC-DC current control achieves all primary design objectives within the 0.2-second simulation window. The Simulink model visible in Fig. 1 confirms the modular architecture, with the power stage (Grid → Filter → FEC → DC-DC → Battery) cleanly separated from the control layer (FEC Control Circuit, DC-DC Control Circuit) and monitoring infrastructure (Spectrum Analyzer, Scope, Measurement Panel).

The initial inrush current spike at t = 0 reaching −600 A in the FEC output current arises from the instantaneous pre-charging of the DC bus capacitor bank. In a practical implementation, a soft-start sequence or pre-charge resistor circuit would limit this inrush to protect the converter switches. The measurement panel in Fig. 1 shows the steady-state values after this transient has settled, confirming correct long-term operation.

The HF ripple visible on the battery charging current waveform (Fig. 2, middle-right) represents residual switching ripple of the DC-DC H-bridge after the output inductance filter. Increasing the output inductance value or raising the switching frequency would reduce this ripple. The ripple amplitude should be evaluated against the battery manufacturer's maximum allowable AC ripple current specification to avoid accelerated $LiFePO_4$ cell ageing.

The spectrum in Fig. 3 confirms that the active VOC rectifier eliminates the characteristic harmonic signature of passive rectifiers. This has significant implications for grid integration: the charger does not require an external harmonic filter at the point of common coupling and imposes minimal reactive power demand on the distribution network, reducing infrastructure costs for charging station operators.

VIII. CONCLUSION

This paper has presented the design, modelling, and simulation of a high-power DC fast charger for electric vehicles implemented in MATLAB R2026a with Simulink and Simscape Electrical. The complete Simulink block diagram (Fig. 1) shows the integrated power and control architecture. The two-stage topology—comprising a three-phase VOC active rectifier and an isolated full-bridge DC-DC converter—demonstrates excellent performance across all evaluated metrics. The VOC-controlled FEC achieves stable 800 V DC bus regulation within 20 ms, draws near-sinusoidal current at unity power factor (PF > 0.98), and produces a supply current THD below 3% (Fig. 3), meeting IEC 61000-3-12 and IEEE 519-2022 requirements. The DC-DC PI current controller delivers accurate 100 A constant-current charging (panel: 99.038 A) with stable battery terminal voltage at approximately 935–950 V (Fig. 2), and the battery SoC increases linearly from 20% as expected in CC mode. The estimated output power of approximately 95 kW places this charger in the Level 3 DCFC category suitable for commercial public charging infrastructure.Future work will investigate the CC-to-CV mode transition under extended simulation, inclusion of semiconductor thermal models for efficiency and loss characterisation, bidirectional DC-DC converter topologies for V2G capability, and hardware-in-the-loop (HIL) validation using a real-time simulation target

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