

DESIGN AND ANALYSIS OF A CASCADE-COUPLED DYNAMIC COMPARATOR

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Abstract : Comparators are fundamental building blocks in Analog-to-Digital Converters (ADCs) and various mixed-signal VLSI systems. The comparators speed power consumption and dependability play a major role in these systems performance. Despite being widely used due to their low-voltage operation and straightforward design conventional double-tail dynamic comparators frequently have higher propagation delays and increased power dissipation which restricts their usefulness in high-speed applications. The design and simulation of a cascode cross coupled comparator combined with an NMOS Power Gating Technique are presented in this work. A cascode cross coupled stage is used in the suggested architecture to enhance the latches regenerative action and reinforce the differential signal. Consequently the comparator reduces propagation delay and makes decisions more quickly. An NMOS power-gating transistor is added to the ground path to reduce leakage current during inactive periods further increasing power efficiency. The Cadence Virtuoso environment is used to design and simulate the entire circuit. The comparators switching characteristics output response propagation delay and power consumption are assessed using transient analysis. The suggested design achieves a propagation delay of 20.07 ps and an average power consumption of 47.12 nW according to the simulation results. The suggested architecture offers notable increases in speed and energy efficiency when compared to the traditional comparator. The suggested comparator is a good option for high-speed and low-power applications such as ADCs communication systems digital signal processing circuits and other mixed-signal VLSI designs because of the improved performance achieved by combining the cascode cross-coupled structure and NMOS power-gating technique.

Keywords: Cadence Virtuoso Cascode Cross-Coupled Structure NMOS Power Gating CMOS Technology Propagation Delay Low-Power VLSI and Dynamic Comparator.

I. INTRODUCTION

Digital signal processing biomedical devices mixed-signal VLSI applications and communication systems all make extensive use of analog-to-digital converters (ADCs). Since it directly affects the systems overall speed accuracy and power consumption the comparator is a crucial part of an ADC. As a result creating high-speed low-power comparators is crucial for contemporary VLSI design. The fast operation and low power characteristics of dynamic comparators make them popular. Nevertheless the performance of traditional double-tail dynamic comparators is limited by issues like slower latch regeneration increased propagation delay and leakage power dissipation. The proposed design an NMOS Power Gating Technique to get around these drawbacks. Propagation delay is decreased by the cascode cross-coupled structures improved latch regeneration speed and differential gain. Furthermore the NMOS power-gating transistor reduces static power consumption and leakage current. The Cadence Virtuoso environment is used in the design and simulation of the suggested comparator. The design is appropriate for high-speed and low-power ADCs communication systems and mixed-signal VLSI applications because simulation results show better speed and lower power consumption when compared with traditional comparator architectures.

II. LITERATURE SURVEY

Komala Krishna and Nandakumar [1] proposed a Cascode Cross-Coupled High-Speed Dynamic Comparator in 65 nm CMOS technology. The cascode cross-coupled stage improved differential gain and accelerated latch regeneration, leading to reduced propagation delay and enhanced speed performance. Gao et al. [2] introduced a common-mode insensitive dynamic comparator to improve operation under varying common-mode voltage conditions. The design provided better stability and sensitivity; however, it exhibited higher kickback noise and increased circuit complexity. Khorami and Sharifkhani [3] presented a low-power dynamic comparator aimed at improving energy efficiency. Their design achieved lower power consumption, but its regeneration speed was limited when processing small differential input signals. Schinkel et al. [4] proposed a double-tail latch-type voltage sense amplifier comparator. By employing separate tail transistors for the input and latch stages, the design achieved higher operating speed and lower kickback noise. However, propagation delay remained significant for low input voltage differences. The literature review indicates that considerable efforts have been made to improve comparator performance in terms of speed, sensitivity, and power efficiency. Nevertheless, simultaneously achieving low propagation delay and low power consumption remains a challenge. To address this issue, the proposed Cascode Cross-Coupled Dynamic Comparator is developed to enhance regeneration speed, reduce leakage power, and improve overall comparator performance for high-speed and low-power VLSI applications.

III. RESEARCH METHODOLOGY

The proposed design is developed to achieve high-speed operation and low power consumption in modern mixed-signal VLSI systems. Comparators are critical components in Analog-to-Digital Converters (ADCs), communication circuits, and digital signal processing applications, where fast decision-making and energy efficiency are essential. Conventional dynamic comparators often suffer from increased propagation delay, limited differential gain, and leakage power dissipation, which affect overall system performance. To overcome these limitations, the proposed architecture incorporates a cascode cross-coupled structure along with an NMOS power gating technique.

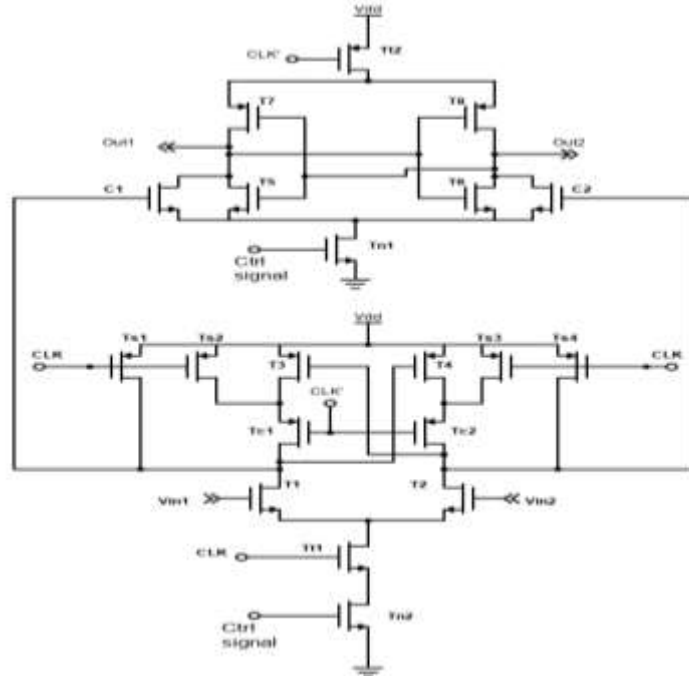


Figure 3.1: circuit diagram of proposed design

The proposed design is composed of four main blocks: the differential input stage, the cascode cross-coupled stage, the regenerative latch stage, and the NMOS power-gating transistor. After receiving the input signals V_{in1} and V_{in2} the differential input stage uses the applied inputs to create a tiny voltage differential at the internal nodes. The first signal for the comparison procedure is this differential voltage. A cascode cross-coupled stage is added between the input and latch stages of the comparator to improve its performance. The voltage difference created at the intermediate nodes is strengthened and the differential gain is increased by this structure. Decision-making is accelerated and propagation delay is decreased because the amplified signal enables the latch to regenerate more quickly. Furthermore the design is appropriate for high-speed and low-power VLSI applications because the enhanced gain improves the comparators capacity to detect minute input voltage variations. The differential voltage generated by the earlier stages is amplified by the regenerative latch stage through the use of positive feedback. In order to create complementary digital outputs during the evaluation phase the latch quickly pushes one output node in the direction of logic high and the other toward logic low. The cascode cross-coupled stage provides a greater voltage difference which speeds up the regeneration process and improves switching performance and response time. An NMOS power gating transistor is integrated close to the comparators ground path to lessen static power dissipation. By regulating the conduction path between the circuit and ground the power gating transistor functions as a sleep transistor. The transistor effectively disconnects the comparator from the ground path and reduces leakage current when it is in standby or inactive. The transistor turns on and permits regular circuit operation when it is in active operation. This method drastically lowers leakage power consumption without negatively impacting operating speed. The precharge phase and the evaluation phase are the two stages of the comparators operation that are managed by a clock signal. The internal nodes are set up and ready for comparison during the precharge stage. The latch regenerates the output to the appropriate logic state after the differential input signals are amplified during the evaluation phase. The comparators improved differential gain quicker regeneration shorter propagation delay and lower power consumption are all made possible by the combination of the cascode cross-coupled structure and NMOS power gating technique. The Cadence Virtuoso environment was used to design and simulate the suggested architecture. According to simulation results the suggested comparator outperforms the traditional comparator with a propagation delay of 20.07 ps and an average power consumption of 47.12 nW. For high-speed and low-power ADCs communication systems and mixed-signal VLSI applications the suggested Cascode Cross-Coupled Dynamic Comparator with NMOS Power Gating Technique is a good option.

3.1 CIRCUIT DESIGN AND SIMULATION

3.1.1 PROPOSED COMPARATOR DESIGN

The existing dynamic comparator was designed and simulated using Cadence Virtuoso in 45 nm CMOS technology. The circuit comprises a differential input pair, regenerative latch, precharge transistors, and clock-controlled switching devices. The comparator operates in two distinct phases: the precharge phase and the evaluation phase.

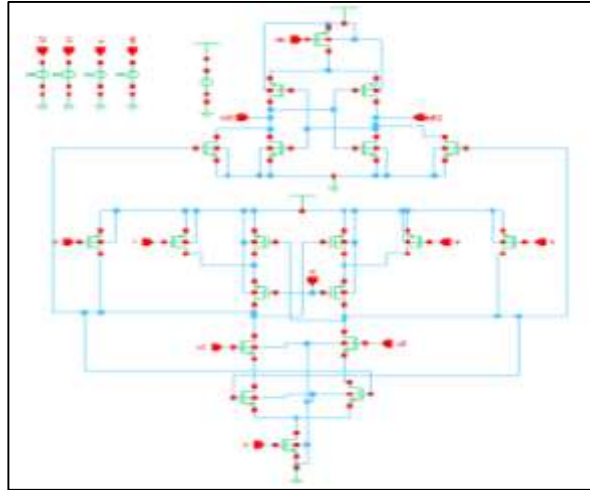


Fig 3.2: Schematic of the existing comparator

Figure 3.2 illustrates the transistor-level design of the existing comparator. During the precharge phase, the output nodes are charged to the supply voltage through the precharge transistors, thereby establishing the initial operating condition for the comparison process. In the evaluation phase, the differential input pair senses the voltage difference between the input signals and converts it into differential currents. The regenerative latch then amplifies the voltage difference through positive feedback, producing complementary digital outputs. Although the existing comparator performs the comparison operation successfully, its performance is constrained by propagation delay, power consumption, and regeneration speed. These limitations motivated the development of an improved comparator architecture. The differential input transistors perform the comparison function, while the cross-coupled latch transistors provide regenerative feedback for output amplification. The comparator converts an analog input difference into a full-swing digital output suitable for high-speed digital processing applications.

3.1.2 Proposed Comparator Design

The proposed architecture retains the advantages of dynamic operation while reducing propagation delay and improving decision accuracy. Furthermore, the cascode configuration improves node isolation and minimizes unwanted signal disturbances during the comparison process.

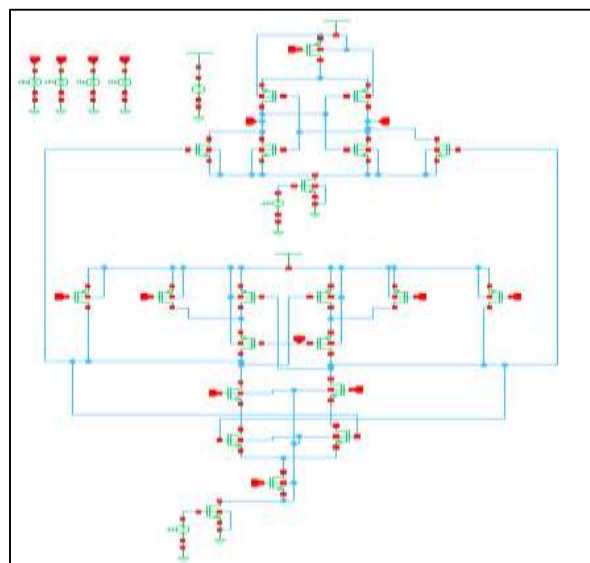


Fig 3.3 : Schematic of proposed comparator

Figure 3.3 presents the transistor-level schematic of the proposed design. The circuit consists of differential input transistors, cascode devices, regenerative cross-coupled latch transistors, and clock-controlled switches. The differential input stage converts the voltage difference between the input terminals into current variations, while the regenerative latch rapidly amplifies these variations through positive feedback. During the evaluation phase, even a small differential input voltage causes one output node to discharge faster than the other. The cross-coupled structure accelerates the regeneration process and produces a clear digital decision at the output nodes. Consequently, the proposed design achieves improved speed and lower delay compared with the conventional comparator architecture.

3.2 Layout Design

After successful verification of the schematic through transient simulation, the physical layout of the proposed design is designed using the Cadence Virtuoso Layout Editor. Layout design converts the schematic into a physical structure that can be fabricated on a semiconductor chip. Proper layout design is important because it affects the area, speed, power consumption, and reliability of the circuit.

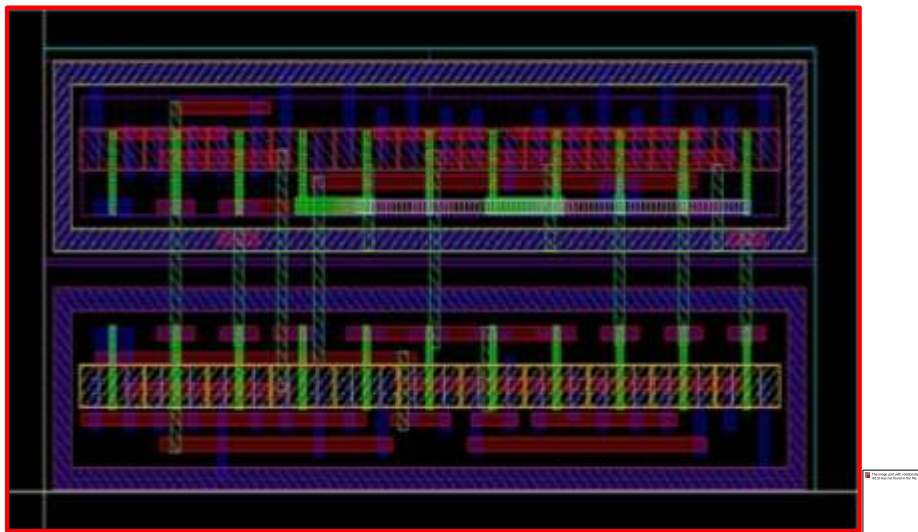


Fig 3.4 : Layout of proposed comparator

Figure 3.4 shows the layout of proposed comparator where it is created by placing PMOS and NMOS transistors according to CMOS design rules. The differential input transistors were placed symmetrically to improve matching and reduce offset errors. The cascode cross-coupled transistors were positioned close to the differential stage to reduce routing complexity and parasitic capacitances. Special care was taken to maintain symmetry between the two branches of the comparator to ensure balanced operation. Metal layers were used for signal routing, power distribution, and ground connections. Routing paths were kept as short as possible to reduce parasitic resistance and capacitance, which can affect circuit speed and power consumption. Proper power and ground rails were provided throughout the layout to ensure reliable operation. The NMOS power gating transistor was placed near the ground path of the comparator. This transistor acts as a sleep transistor and helps reduce leakage current during standby conditions, thereby lowering static power consumption. Appropriate spacing and contact structures were provided to satisfy fabrication requirements and improve circuit reliability. The completed layout was optimized to minimize parasitic effects and maintain the performance achieved at the schematic level. The final layout provides a compact, reliable, and fabrication-ready implementation of the proposed comparator.

IV. RESULTS AND DISCUSSION

4.1 Transient Analysis of Existing Comparator

The transient waveform illustrates the operation of the comparator during the precharge and evaluation phases. During precharge, the output nodes are charged to the supply voltage level. When the clock enters the evaluation phase, the comparator starts comparing the differential input signals. Based on the input polarity, one output node discharges while the complementary output remains near the supply voltage. The regenerative latch amplifies the voltage difference and produces a valid digital output. Although the comparator operates correctly, the observed output transition delay highlights the need for further performance improvement.

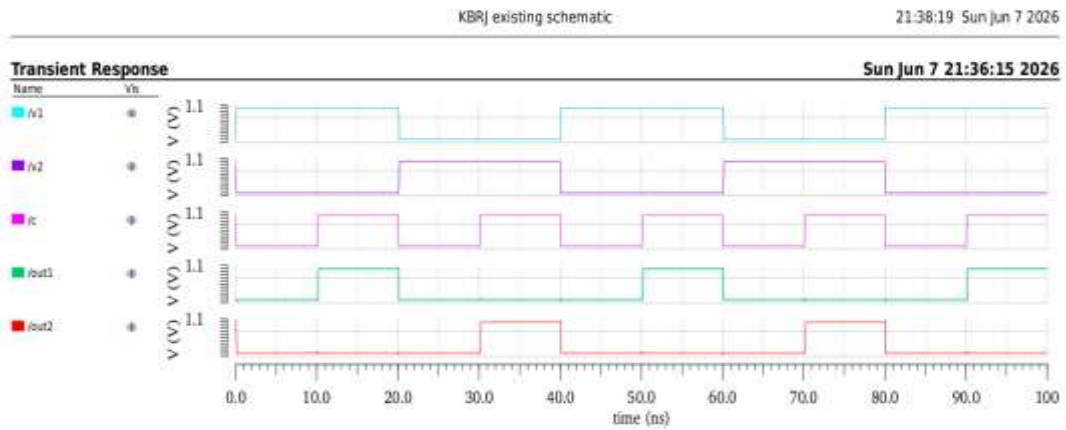


Fig 4.1 : Waveform of Existing Method

4.2 Transient Analysis of Proposed Comparator

Transient analysis was also performed on the proposed design under identical operating conditions to evaluate the performance improvement achieved through the modified architecture. The transient waveform verifies that the suggested Cascode Cross-Coupled Dynamic Comparator is operating correctly. Both output nodes are charged to the supply voltage during the precharge phase. The differential input pair detects the input voltage difference and starts the comparison process as soon as the evaluation phase begins. Through strong positive feedback the cascode cross-coupled latch quickly regenerates the differential signal resulting in a full-swing digital output. The suggested design outperforms the current comparator in terms of regeneration speed propagation delay reduction and output transition speed. The simulation results unequivocally show how well the suggested architecture improves comparator performance while keeping power consumption low.

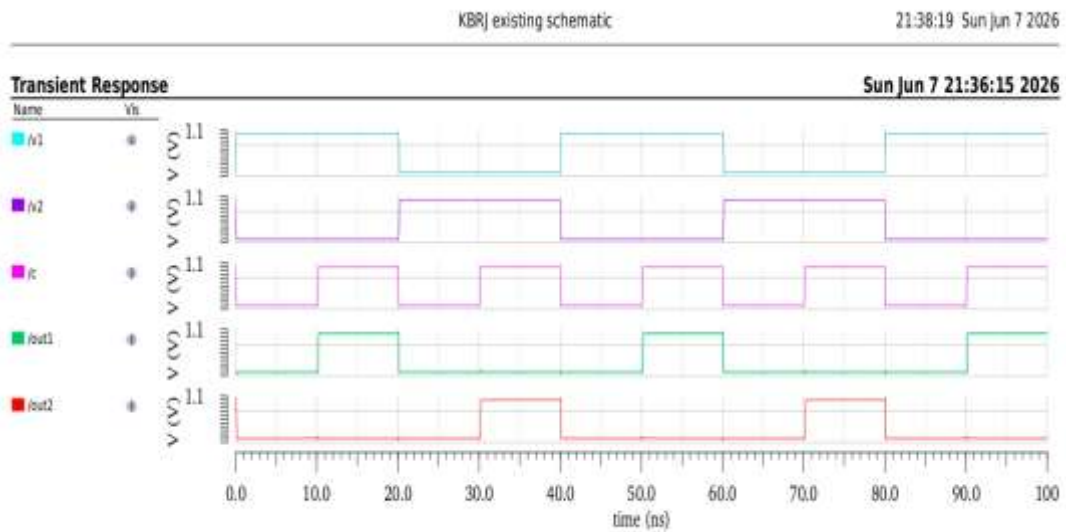


Fig 4.2 : Waveform of Cascode Cross-Couple Dynamic Comparator

The **propagation delay** measurements were obtained using transient analysis in the Cadence Virtuoso simulation environment. The delay was measured between the transition of the input signal and the corresponding transition of the output signal. The simulation results indicate that the existing comparator exhibits a propagation delay of **51.04 ps**, whereas the proposed Cascode Cross-Coupled Double Tail Dynamic Comparator achieves a delay of only **20.07 ps**.

Thus, the proposed comparator achieves approximately **60.68% reduction in propagation delay** compared to the existing architecture. The significant reduction in delay demonstrates the effectiveness of the proposed cascode cross-coupled structure in improving regeneration speed. Faster regeneration increases the comparators overall speed and permits quick output transitions. The comparator can function effectively at higher frequencies due to the decreased delay which makes it appropriate for contemporary high-performance VLSI systems. Cadence Virtuoso simulation tools were used to determine the average power consumption of the two comparator architectures. According to the simulation results the suggested comparator uses just 47.12 nW of power while the current comparator uses an average of 90.19 nW. As a result the suggested comparator reduces average power consumption by about 47.75 percent when compared to the current comparator. The NMOS power gating transistor which successfully suppresses leakage current during inactive periods is primarily responsible for the decrease in power consumption. Reduced power consumption lowers the circuits thermal stress and increases energy efficiency. Because of this the suggested comparator is ideal for low-power VLSI designs wireless communication systems portable electronics battery-operated devices and Internet of Things applications. The efficacy of the suggested design is demonstrated by the combined reduction in delay and power consumption. While the NMOS power gating method minimizes leakage current and lowers power dissipation the cascode cross-coupled structure

enhances differential gain and regeneration speed leading to a lower propagation delay. Therefore the suggested Cascode Cross-Coupled Double Tail Dynamic Comparator is a good option for next-generation mixed-signal and digital integrated circuits since it offers a balanced combination of high-speed performance and low-power operation.

4.3 Performance Comparison

To evaluate the effectiveness of the proposed Cascode Cross-Coupled Dynamic Comparator, its performance was compared with that of the existing comparator. Key performance parameters such as propagation delay and power consumption were analyzed under identical operating conditions.

Table 4.1 Performance Comparison of Existing and Proposed Comparator

Parameters	Existing Method	Proposed Method
Delay	51.04 ps	20.07 ps
Average Power Consumption	90.19 nW	47.12nW
Mos Count	20	22

The comparison results show that the proposed comparator performs better than the existing design. The cascode cross-coupled structure improves regeneration speed, enabling faster decision-making and reducing propagation delay. In addition, the optimized architecture lowers power consumption, resulting in an improved Power-Delay Product (PDP). These enhancements make the proposed comparator suitable for high-speed and low-power VLSI applications.

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