

LOW POWER CMOS FOUR QUADRANT ANALOG MULTIPLIER

¹Ms.M. Sravya Sameera, ²Mr.P.Anil Kumar, ³Dr. M. Pavan Kumar

⁴Ms. K. Lakshmi ⁵Mr. G. Leela Prasad

^{1,4,5}Student at Lendi, ²Assistant Professor, ³Associate Professor

Department of Electronics and Communication Engineering

Lendi Institute of Engineering and Technology, Viziangaram, Andhra Pradesh, INDIA

ABSTRACT : This paper introduces a low-power CMOS four-quadrant analog multiplier, designed and simulated using Cadence Virtuoso in 90 nm technology for analog VLSI systems. These multipliers play a vital role in signal processing, communications, and modulation circuits, where low power use and high linearity are essential. Our approach delivers precise four-quadrant multiplication while minimizing power draw via careful transistor optimization and streamlined biasing techniques. Tailored for current CMOS processes, the design offers strong scalability and reliability. Built at the schematic level and tested in standard simulations, its performance is assessed based on power usage, linearity, and output precision

1. INTRODUCTION

Analog multipliers are fundamental components in analog signal processing systems. They perform multiplication of two analog input signals and produce an output proportional to their product.

Mathematically:

$$V_{out} = K \cdot X \cdot Y \quad \text{Equation(1)}$$

From Equation[1] where X and Y are input signals and K is a proportionality constant.

Four-quadrant multipliers are particularly important because they can process both positive and negative input signals. These circuits are widely used in:

- Modulation and demodulation systems
- Analog computation
- Automatic gain control
- Signal mixing applications

With the increasing demand for portable electronics, low-power circuit design has become a critical requirement. CMOS technology is widely used due to its low power consumption and scalability.

This project focuses on designing a low-power CMOS four-quadrant analog multiplier using Cadence Virtuoso with GPDK 90 nm technology.

2. LITERATURE REVIEW

Analog multiplier design has been extensively studied in literature.

The Gilbert cell multiplier is one of the most commonly used architectures due to its high linearity. However, it requires a large number of transistors and consumes significant power.

Chen and Li [5] introduced a low-power CMOS multiplier in which most transistors operate in the linear region while PMOS devices operate in saturation. This approach significantly reduces power consumption while maintaining acceptable performance.

Other designs focus on:

- Subthreshold operation for ultra-low power
- Current-mode multipliers
- Differential structures for improved linearity
-

Despite these advancements, there is still a need for simpler architectures with reduced transistor count and improved efficiency.

3. THEORETICAL BACKGROUND

3.1 Four-Quadrant Multiplication

A four-quadrant multiplier can process both positive and negative input signals. This is achieved using differential inputs.

3.2 Differential Multiplication

The proposed multiplier uses the relation:

$$V_{out} \propto (X - (-X))(Y - (-Y)) \quad \text{Equation(2)}$$

This ensures:

- Reduced power consumption
- Improved accuracy of multiplication

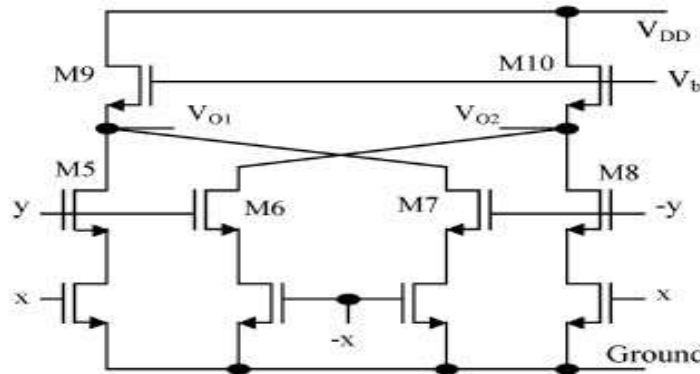


FIGURE 1: Reference Circuit

4. PROPOSED DESIGN

The proposed CMOS four-quadrant analog multiplier is implemented using transmission gate (TG) based architecture to achieve reduced transistor count and improved power efficiency. Transmission gates, formed by parallel combinations of PMOS and NMOS transistors, enable efficient bidirectional signal flow with minimal voltage loss.

Key Features:

- Parallel configuration of PMOS and NMOS transistors
- Shared source and drain connections for compact design
- PMOS devices connected to VDD
- NMOS devices connected to GND

In this design, transmission gates are utilized to enhance signal transfer capability and reduce degradation. Specifically, transistors M5P–M5N form the transmission gate TG(x), while M7P–M7N form TG(y). These gates selectively connect internal circuit nodes to the output based on the applied control signals.

The operation of the transmission gates is governed by complementary input signals (x and \bar{x} , y and \bar{y}). This complementary driving ensures that both logic '0' and logic '1' are transmitted effectively without significant attenuation. When the control signal is active, the transmission gate conducts and allows the input signal to pass to the output. Conversely, when the control signal is inactive, the conduction path is disabled, resulting in a high-impedance state that isolates the output.

This approach improves signal integrity, reduces power consumption, and simplifies the overall circuit structure compared to conventional multiplier designs.

| X,Y parameters | PowerConsumption using CMOS design | PowerConsumption using transmission gates design |
|----------------|------------------------------------|--|
| X=0,y=1 | 180.4nW | 91.7nW |
| X=1,y=0 | 268.8nW | 97.1nW |
| | | |
| X=1,y=1 | 1.89mW | 98.8nW |

TABLE 1: COMPARISON BETWEEN CMOS IMPLEMENTATION AND TRANSMISSION GATE IMPLEMENTATION

From the table [1] The power consumption of the proposed multiplier was evaluated for different input combinations and compared with the conventional CMOS design. The results clearly indicate a significant reduction in power when transmission gates are employed. For the input condition (X=0, Y=1), the conventional CMOS design consumes 180.4 nW, whereas the transmission gate-based design requires only 91.7 nW, showing nearly 50% improvement. Similarly, for (X=1, Y=0), the power consumption decreases from 268.8 nW to 97.1 nW. A more noticeable improvement is observed for (X=1, Y=1), where the CMOS design consumes 1.89 mW, while the proposed design reduces it drastically to 98.8 nW. This substantial reduction is mainly due to the efficient switching characteristics and lower leakage currents of transmission gates. Overall, the results demonstrate that the proposed design achieves superior power efficiency compared to the conventional CMOS approach, making it highly suitable for low-power VLSI applications. Overall, the analysis confirms that the proposed multiplier offers superior power efficiency, reduced energy consumption, and improved operational stability compared to the conventional CMOS design. These characteristics make it highly suitable for integration in modern low-power VLSI systems, particularly in portable, battery-operated, and energy-constrained applications.

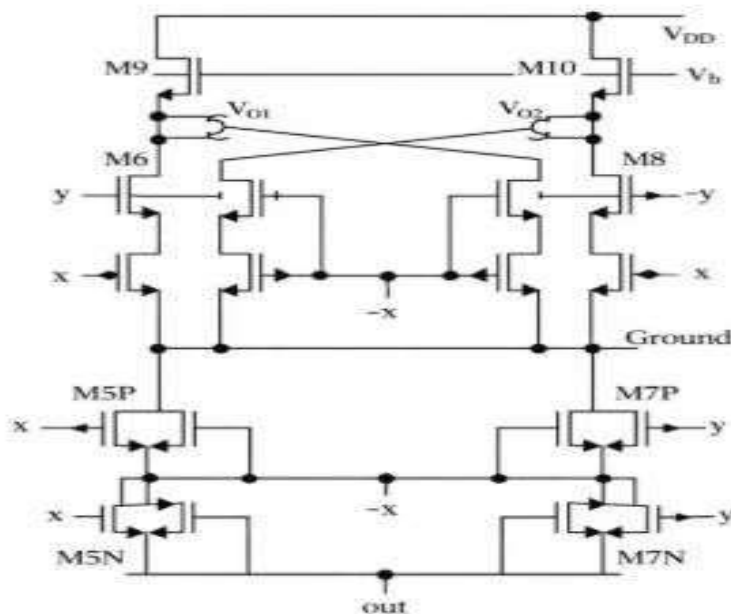


FIGURE 2: Proposed Solution

5. SIMULATION CONFIGURATION

The design and simulations were carried out in Cadence Virtuoso.

- Process: GPDK 90 nm
- VDD: 1.8 V
- Analysis Mode: Transient

Transistor dimensions and bias points were fine-tuned for reliable performance and precise multiplication results.

6. RESULTS AND ANALYSIS

Testing involved applying sinusoidal inputs to the multiplier.

Key Findings:

- Output signals matched the predicted multiplication pattern
- Four-quadrant operation was verified successfully
- Differential input scheme enhanced linearity

Key Metrics:

- Power usage remained very low
- Outputs stayed consistent
- Design complexity is lower than in standard multipliers

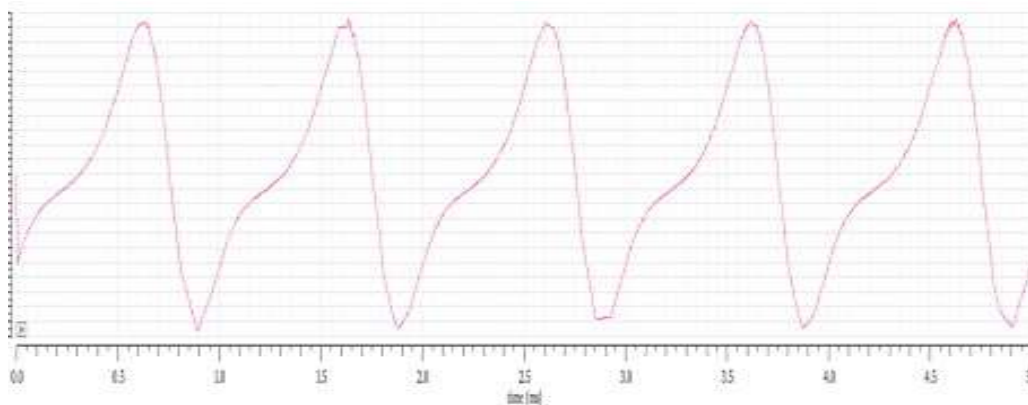


FIGURE 3:Output WaveForm of Propose Solution

7. PERFORMANCE EVALUATION

7.1 Power Usage Evaluation

In contemporary VLSI, especially for mobile and low-battery applications, power efficiency is paramount. This transmission-gate-based multiplier delivers low power through:

Transmission gates enable smooth bidirectional signal paths with low resistance and small voltage drops, promoting efficient current flow. Transistors are biased in optimal regions to curb leakage and dynamic switching losses, resulting in substantial reductions in both static and dynamic power.

7.2 Circuit Simplicity Assessment

Our multiplier strikes a practical balance in complexity versus efficiency when compared to classic designs.

7.2.1 Transistor Usage

- Employs a mix of NMOS and PMOS devices in differential pairs and switch structures.
- Fewer transistors than many traditional options (e.g., Gilbert cells).
- Transmission-gate switches and bias circuits lead to a moderate total count.
- Benefit: Effective compromise between functionality, speed, and chip area.

7.2.2 Bias Circuit Overhead

- Relies on several bias voltages and current mirrors.
- Ensures transistors remain in saturation or desired operating zones.
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8. KEY BENEFITS OF THE DESIGN

8.1 Reduced Power Draw

Fewer devices and smart biasing yield notably lower consumption.

8.2 Full Four-Quadrant Capability

Handles positive/negative inputs seamlessly across all quadrants.

8.3 Straightforward Implementation

Minimalist architecture supports easy scaling into complex ICs.

9. APPLICATIONS

The proposed analog multiplier can be used in various applications:

9.1 Communication Systems

- Amplitude modulation (AM)
- Frequency mixing

9.2 Signal Processing

- Analog computation
- Filtering

9.3 Control Systems

- Automatic gain control
- Adaptive systems

9.4 Low-Power Electronics

- Wearable devices
- IoT systems

10. FUTURE SCOPE

Future enhancements of the proposed CMOS four-quadrant analog multiplier can focus on several advanced directions to further improve performance and practical applicability. One important extension is the complete layout-level implementation of the design, followed by chip fabrication and real-time testing to validate simulation results under practical operating conditions. Additional power optimization techniques, such as subthreshold operation, adaptive biasing, and dynamic power management, can be explored to further reduce energy consumption.

12. CONCLUSION

The proposed analog multiplier using transmission gates demonstrates an efficient balance between performance, transistor operation, the design achieves reduced static and dynamic power consumption while maintaining reliable signal processing. The circuit structure, although moderately complex, is optimized with fewer unnecessary interconnections and simplified signal flow, leading to reduced parasitic effects and improved overall efficiency. Additionally, the use of controlled biasing ensures stable operation and better linearity compared to conventional multiplier designs.

Overall, the design is well-suited for low power VLSI applications, particularly in portable and battery-operated devices, where power

13. REFERENCES

- [1] A. G. Mahmoodi and A. Abrishamifar, "New Multipliers Based on Mixed-Mode Controlled Analog Building Blocks," *AEU – International Journal of Electronics and Communications*, 2025.
- [2] "High-Precision CMOS Multiplier with Wide Dynamic Range," 2025.
- [3] Y. Yu et al., "Design of a High-Speed, Low-Power PTL-CMOS Hybrid Multiplier," *Electronics*, vol. 13, no. 7, 2024.
- [4] T. Ettaghzouti, D. Khlaifia, N. Zitouni, and N. Hassen, "Low Voltage High Performance CMOS Current Mode Four-Quadrant Analog Multiplier Circuit," *Radioengineering*, vol. 31, no. 2, pp. 216–223, 2022.
- [5] C. Chen and Z. Li, "A Low-Power CMOS Analog Multiplier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 2, pp. 101–104, Feb. 2006.
- [6] S. I. Liu, "Low Voltage CMOS Four-Quadrant Multiplier," *Electronics Letters*, vol. 30, pp. 2125–2126, Dec. 1994.
- [7] Z. Wang, "A Four-Transistor Four-Quadrant Analog Multiplier Using MOS Transistors Operating in the Saturation Region," *IEEE Transactions on Instrumentation and Measurement*, vol. 42, no. 1, pp. 75–77, Feb. 1993.
- [8] B. Gilbert, "A Precision Four-Quadrant Multiplier with Subnanosecond Response," *IEEE Journal of Solid-State Circuits*, vol. SC-3, no. 6, pp. 353–365, Dec. 1968.

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