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7-Transistor SRAM by using 45nm Technology in conjunction with the Tanner Tool to lessen the power

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Abstract - The chip design industry is under increasing pressure to decrease power consumption in electronic circuits and, by extension, prolong battery life, to meet the rising demand for portable electronic devices and systems powered by batteries. CMOS SRAM memory contributes around 60 % of the total power consumption in the digital circuit. Memories are seen as power-hungry elements in digital systems; however, they have become essential in modern digital sys tems. This article analyses the rationale for decreasing the dynamic power con sumption of SRAM memory. The size, latency, and power dissipation of the 45 nm 7 transistor SRAM memory cell are evaluated using the Tanner tool. The article delves into the topic of electrical energy loss due to switching and short circuits. A 45nm manufacturing process is used by the circuit, which operates on a 1.0-volt supply and has a 0.3-volt threshold voltage.
Index Terms - Power dissipation, 45nm Fabrication process, CMOS SRAM, Digital systems.

1. Introduction (Heading 1)

The write mode of an example SRAM cell is shown in Figure 1. During a write opera tion, the phrase "word line" is used to activate the access transistors M1 and M2. The data and its complement may be stored using BL and *BL* line. When performing a write operation to a memory location, one of the bit lines is set to a high voltage while the other is maintained at a low value. Figure 1 depicts a conventional 6T SRAM cell, as cited in reference [1]. The memory architecture is distinguished by its asynchronous random-access design. This statement is founded on the concept that addresses, which are segments of memory, may be accessed for reading or writing in a non-sequential manner at a consistent pace, irrespective of their physical location. The storage array, known as the core, consists of fundamental cell circuits arranged in a grid-like design to maximise the efficient sharing of connections in both the horizontal and vertical di rections. The term "lines" refers to the horizontally controlled lines in the storage array, whilst "bit lines" refer to the vertical lines that cells use for data input and output. Choosing the correct row and column is crucial for accessing or modifying cell data. Any cells may hold the binary numbers 0 and 1. The programme calculates the upper limit of columns that memory may allocate in a single row, ranging from 4 to 64. The possible options consist of the numbers 4, 8, 16, 32, and 64. Analysing the binary ad dress data allows us to determine the specific row and column (or sets of columns). Let's examine a row decoder that has a total of 2n output lines. A binary input code of n bits defines the activation status of the lines. The column decoder's 2 m bit line access signals allow for the activation of any one of the m inputs simultaneously. A multiplexer circuit is used to choose certain bits and direct their cor responding cell outputs to data registers. The total number of cells in the core array is equal to the product of 2 raised to the power of n and 2 raised to the power of m. This design's symmetrical 64-unit rows and columns result in a decrease of 4 MB of RAM. An 8 MB static random access memory (SRAM) may be constructed by merging two memory slices. An SRAM IC, or Static Random Access Memory Integrated Circuit, is a kind of circuit that enables the storage and retrieval of data bits inside a memory array. The SRAM IC was constructed using the CDS IC446 design environment from Ca dence. This pattern was derived from the AMI 0.6-micron technique. The architecture of the SRAM IC consists of a row decoder, sense amplifiers, multiplexers, NAND gates, AND gates, NOR gates, and SRAM cells. The cell is a crucial component since it serves as a core link for several circuits. The SRAM memory array was developed using the widely-used CMOS 6 transistor cell design [2]. The all-encompassing CMOS SRAM architecture has many advantages, including compatibility with high-density SRAM arrays, rapid switching speeds, low static power consumption, and excellent noise tolerance. A 64-bit SRAM was constructed by using 64 fully integrated CMOS 6-T cells. A solitary bit may be saved using a solitary CMOS 6-T cell [10]. In our literature research, we found that substantial progress has been made in reducing dy namic power dissipation. In addition, we have come across a study article that provides a comprehensive analysis of static power dissipation. With the advancement of tech nology, power dissipation has emerged as the paramount consideration in the construc tion of SRAM memory. When it comes to the total amount of power being released, memory is the most dominant. By conducting a thorough examination of the current literature and assessing earlier research, we were able to effectively minimize power loss caused by short circuits in SRAM memory cells. Our literature investigation re vealed that SRAM memory cells use a significant amount of short-circuit power during input data transition phases. This occurs due to a direct electrical connection between the V dd and ground at specified intervals. By

using 45 nm technology, the short circuit power inside a single cell decreases to a level below the micro-watt barrier. The size of memory is closely correlated with power usage. Based on our analysis of the literature, we have decided to improve the efficiency of the short-circuit power. In most system on-a-chip (SOC) architectures, embedded memory—also called static random access memory (SRAM)—consumes the most power and occupies the most space. To sustain performance, it is necessary to reduce the thickness of the transistor oxide layer proportionally, ensuring sufficient current flow even at reduced supply voltages. By disabling the stack transistors while the memory is not in use, the leakage current is further reduced by using the stacking effect. The lowering of transistors has led to a substantial drop in battery life and an increase in leakage currents. The objective of low-power reduction solutions is to minimise leakage. These solutions investigate the correlation between tunneling currents and terminal voltages, gate oxide thickness, and the kind of transistor. Several efficient methods surpass the current cutting-edge SRAM design methodologies. At the 45 nm technological nodes, these techniques allow the examination and replication of several factors. They effectively prioritise efficiency in circuit size, speed, temperature sensitivity, and power dissipation.

2. CALCULATION OF CMOS CIRCUITS' POWER USAGE

The power consumption of digital CMOS VLSI circuits may be ascribed to three main components. 1) Power Switching: The power used when the transistor switches and charges or discharges the capacitances in the circuit. When a current flow short-circuit from the power source to earth while a transistor is being switched, this phenomenon is called short-circuit power. This feature is quickly becoming standard in DSM technol ogy. A circuit's static power is the amount of electrical power it draws while it is oper ating in a steady state, due to static and leakage currents. Since power is always being used throughout the state changes of the circuit, the first two components are called dynamic power. Digital CMOS VLSI circuits operating at the nanotechnology level mostly rely on dynamic power to power themselves.[15], [16]. The power consumption of digital CMOS VLSI circuits may be ascribed to three main components. 1) Power Switching: The power used when the transistor switches and charges or discharges the capacitances in the circuit. short-circuit power: A short-circuit current wastes electricity when it flows from the power source to ground during a transistor's switching process. Deep Sub Micron (DSM) technologies are starting to include this functionality more often. Static power: the power used by a circuit due to static and leakage currents while the circuit is in a stable state. The first two components are referred to as dynamic power since power is actively used throughout the circuit's state shifts. The primary factor responsible for the total power consumption in digital CMOS VLSI circuits at the nan otechnology level is dynamic power [15], [16].

3. Layout of a Low Power SRAM Cell

During writing, a low power SRAM cell operates in the way shown in Figure 2. When writing, the term "word line" is used to start the access transistors M1 and M2 working. The storing of data and its complement is accomplished using bit lines (BL) and word lines. A write operation involves driving one bit line (BL) to a high voltage level and keeping the other bit line at a low voltage level. We have included an additional tran sistor that serves as a control signal to ensure that the transistors in low power SRAM cells are efficiently regulated.

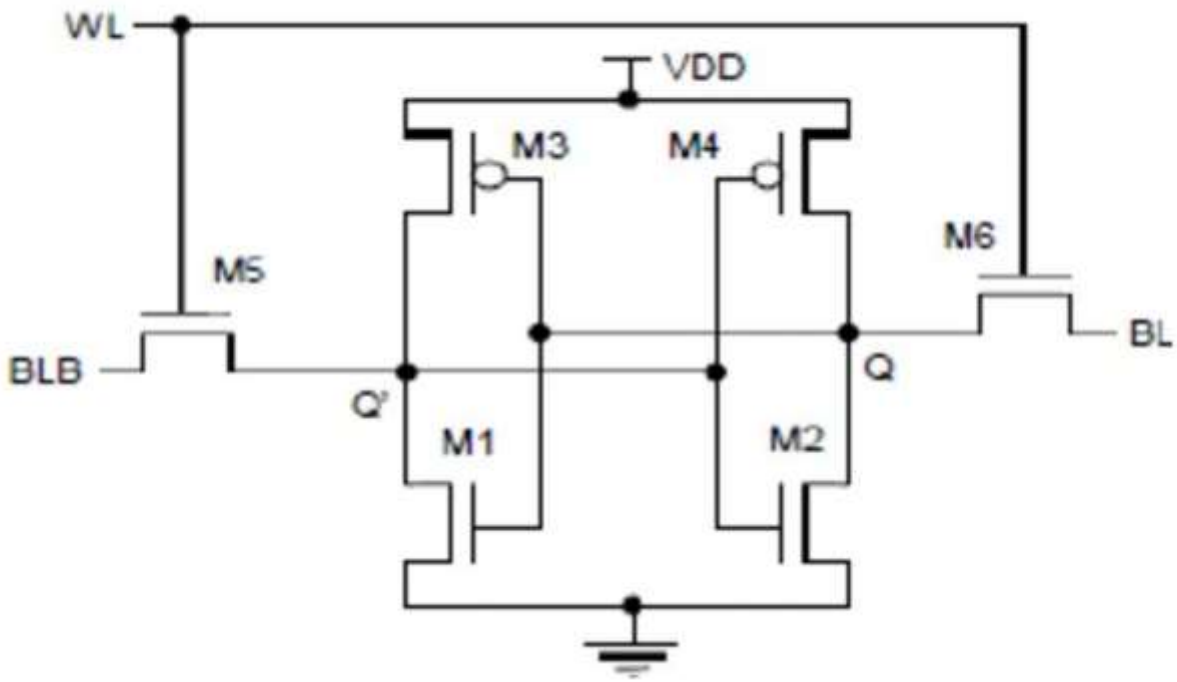

Fig. 1. The Standard 6T SRAM Module

Adding a transistor does increase the low-power SRAM cell's surface area compared to the conventional method. The control chooses signals that allow this transistor to effec tively regulate the power consumption caused by short circuits. This transistor receives a control signal during a writing operation and operates in a "on" state. Keeping it in the off state is necessary while the read operation is running. When turned off, this transistor will interrupt the zero-voltage electrical connection between Vdd and Ground. Figure 3 displays circuit

schematics of SRAM cells with low power consump tion.

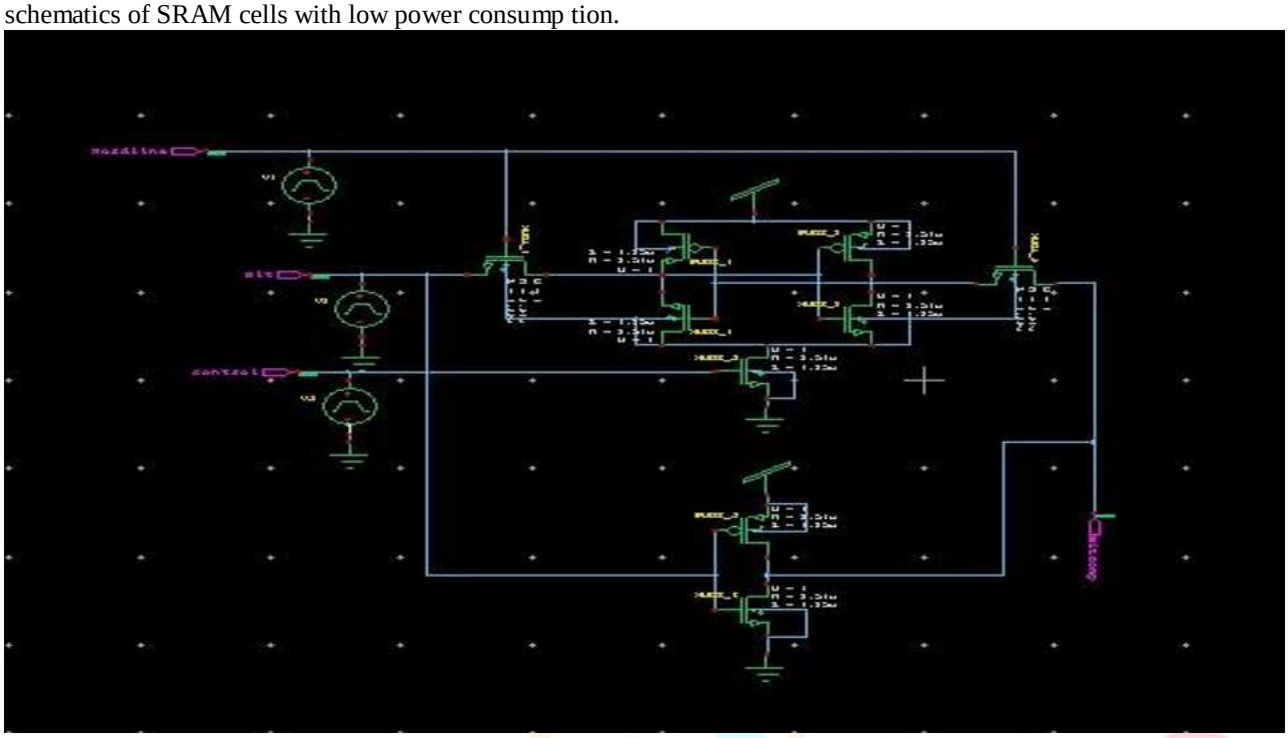

Fig. 2. Low Power SRAM Cell

The delay is a critical attribute of the SRAM cell. The performance of SRAM in high-speed applications is dictated by the delay experienced during read-and-write op erations. Delay is the duration between the rising and falling times of a pulse. The com putation may be performed using horizontal and vertical lines inside the EDA TANNER software. The power dissipation may be modified by altering the width of the transistor. When the width value is at its minimum, we see the quantity of power that is being squandered. The average power is the sum of the short circuit power and the switching power.

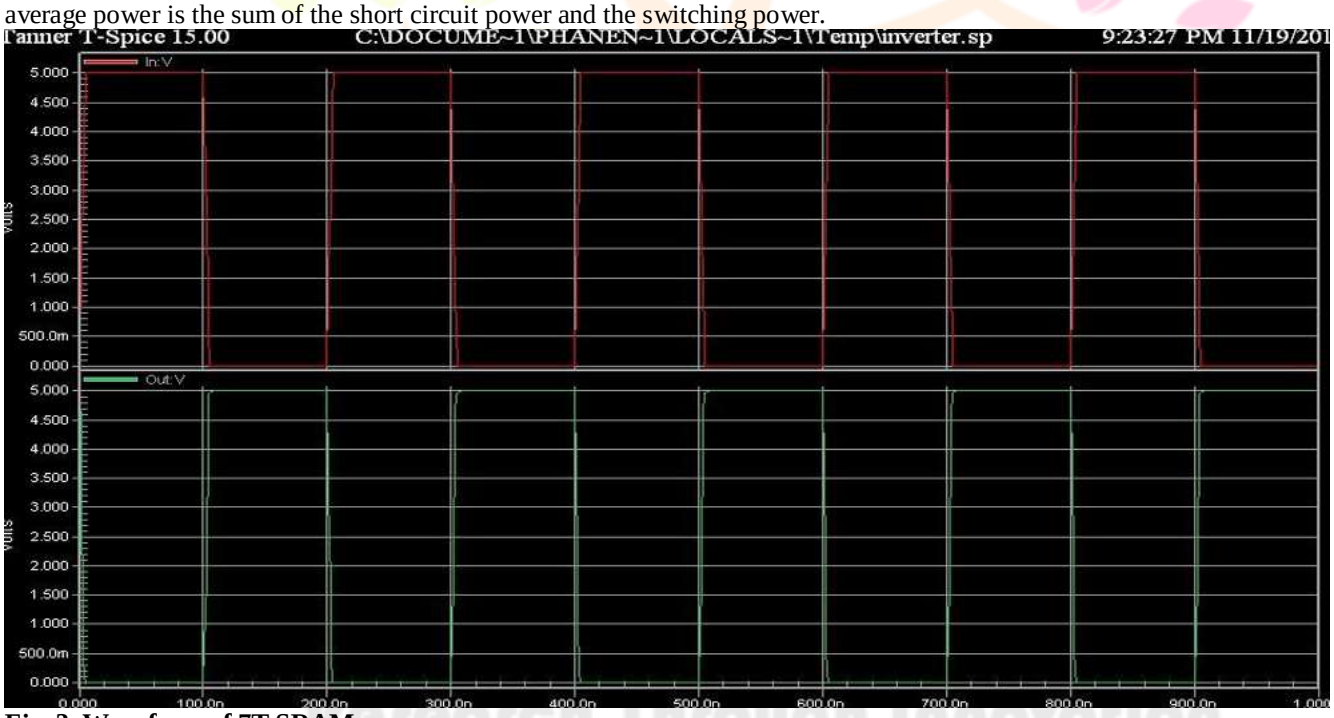

Fig. 3. Waveform of 7T SRAM.

Dynamic energy consumption is the quantity of energy used by the power supply while performing read and write operations. Furthermore, it affects the length of time that a battery may function in mobile apps. The power consumption has been lowered to 0.4 units.Table I provides the power The power dissipation is 4.68 w at a width of 0.5 µ. The value of power dissipation for a 7-transistor SRAM cell is shown in Table 1. Evidence suggests that power dissi pation drops in direct proportion to cell diameter. The power dissipation also reaches its minimum when the value of w hits its lowest point, which is at w = 0.2µ.

Table 1. Table captions should be placed above the tables.

Width(μ)	W=0.2μ	W=0.3μ	W=0.4μ	W=0.5μ
Power dissi-pation(μW)	P=4.251w	P=4.247w	P=4.633w	P=4.682w

4. conclusions

This article details the implementation of a modified model that improves processing speed and power efficiency by using an efficient SRAM memory cell and other tech niques to reduce power consumption. The issues caused by high temperatures may be mitigated by cutting down on electricity use. Reduced temperatures on the device also lessen stress gradients, which improves the system's durability. Devices that use batter ies have their battery life increased, which is another advantage of lower power use. A lower quantity of power dissipation is shown by the investigation.

5. References

1. Upadhyay and Mr. Rajesh Mehra, "Low Power Design of 64-bits Memory by using 8-T Proposed SRAM Cell", International Journal of Research and Reviews in Computer Science (IJRRCS), Vol. 1, No. 4, December 2010.
2. Sreerama Reddy G.M, P. Chandrashekara Reddy, "Design and VLSI Implementation of 8 Mb Low Power SRAM in 90nm", European Journal of Scientific Research ISSN 1450 216X, Vol.26 No.2 (2009), pp.305-314.
3. eejong Kim, Hamid Mahmoodi, "A Low-Power SRAM Using BitLine Charge-Recycling", IEEE Journal of Solid State circuits, Vol 43, no. 2, Feb 2008.
4. Yung-Do Yang and Lee-Sup Kim, "A Low-Power SRAM Using Hierarchical Bit Line and Local Sense Amplifiers" IEEE Journal of solid state circuits, Vol.40, No. 6, June 2005.
5. Chang, Y., Lai, F. and Yang, C., "Zero-aware asymmetric SRAM cell for reducing cache power in writing zero", IEEE Trans. VLSI Systems, Vol. 12, no. 8, pp. 827-36,2004.
6. Aly, R., Faisal, M. and Bayoumi, A., "Low-power cache design using 7T SRAM cell" in Proc. IEEE System on Chip Conference, pp. 171-174, 2005.
7. Neil H. E. Weste, David Harris, Ayan Banerjee "CMOS VLSI Design, Pearson Education, third Edition, pp. 55-57.
8. Ken Martin, "Digital Integrated Circuit Design"
9. Varun Kumar Singhal, Balwinder Singh, "Comparative study of power reduction techniques for Static random access memory" International Journal of VLSI and Signal Processing Ap plications, Vol. 1, Issue 2 , May 2011,(80-88) ,ISSN 2231-3133.
10. Irina Vazir, Prabhjot S. Balaggan, Sumandeep Kaur, Cailan Shen, "SRAM IP for DSP/SOC Projects" San Jose State University SRAM.
11. Ashish Siwach, Rahul Rishi," IJCEM International Journal of Computational Engineering Management, Vol. 11, January 2011.
12. Texas Instruments, "CMOS Power Consumption and Cpd Calculation" SCAA035B June 1997.
13. Debasis Mukherjee, Hemanta Kr. Mondal and B.V.R. Reddy, "Static Noise Margin Analysis of SRAM Cell for High Speed Application" IJCSI International Journal of Computer Sci ence Issues, Vol. 7, Issue 5, September 2010.
14. Shilpi Birla, Neeraj Kr. Shukla, Manisha Pattanaik, R. K. Singh,"Device and Circuit Design Challenges for Low Leakage SRAM for Ultra Low Power Applications" Canadian Journal on Electrical & Electronics Engineering Vol. 1, No. 7, December 2010.
15. Benton H. Calhoun, Member, IEEE, and Anantha P. Chandrakasan, Fellow, IEEE, "Static Noise Margin Variation for Sub-threshold SRAM in 65-nm CMOS" IEEE Journal of solid state circuits, vol 41, no.7, july 2006.
16. N.M. Sivamangai and K. Gunavathi, Non-members, "A Low Power SRAM Cell with High Read Stability" ECTI Transaction on electrical engineering, electronics and Communica tion, vol 9, no. 1, 2011.
17. Srinivasa Rao, Raghavendra Sirigiri, V. Malleswara Rao, "New Technique for reducing sub threshold leakage in SRAM" International Journal of Engineering Sciences Research-IJESR may 2011.
18. Massoud Pedram, "Design Technologies for Low Power VLSI".
19. Anantha P. Chandrakasan Robert W. Brodersen, "Minimizing Power Consumption in CMOS Circuits".
20. M. Michael Vai, "VLSI Design (VLSI Circuits)".
21. Sung-Mo (Steve) Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis & Design".
22. Syed Shakib Sarwar, Syed an Nazmus Saqueb, Farhan Quaiyum (student member, IEEE), and A. B. M harun-ur rashid (Senior Member, IEEE), " Memristor Based Nonvolatile Ran dom Access Memory: Hybrid Architecture for Low Power Compact Memory Design", IEEE, Volume 1, February 3, 2013, accepted April 14, 2013, 2169-3536, published May 10, 2013.