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IP LEVEL VERIFICATION OF ETHERNET PROTOCOL USING WISHBONE INTERFACE

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Abstract: SOC (System- on-a-Chip) is the international VLSI evolution paradigm that's nowadays conquering IC evolution. This document describes the verification of Ethernet MAC (Media Access Control) applying UVM (Universal Verification Approach), the most widely used verification methodology. Ethernet frames are furthered to PHY over MII (Media Independent Interface) by MAC, while frames from PHY are admitted by MAC through the identical interface. An elegant system of validating MAC characteristics, similar as frame transmission and reception, is through IP verification achieves coverage driven verification at its best by exercising factory and configuration mechanisms, coverage measures, and self- checking, which shortens the time needed for design verification.

Index Terms - WISHBONE bus, Media Access Control, Verification Methodology Manual, System Verilog, Assertions, UVM, Verilog.

I.INTRODUCTION

As microelectronics technologies advance, hardware integration levels rise steadily, making it possible to combine a CPU, memory, and I/O device on a single chip. SoC occurs when the need arises and establishes itself as a typical design method for embedded systems because to its high integration, high reliability, and short time-to-market. Currently, there are millions to billions of transistors integrated into a single chip in a single device. The semiconductor industry has started creating intellectual property (IP) cores created by various semiconductor suppliers as hardware designs become more complicated. A system-on- chip is created by combining all of these IP cores for flexible operation. Requirements may be slightly different from specifications while creating an IP core. If deviations are overlooked, even little variances result in inaccuracies in real- world settings. As a result, validation, as opposed to design, is crucial in ensuring the validity of the design and identifying flaws. This may prevent several losses for semiconductor businesses. The future of networking technology is fading away. It might be a wireless or wired network. Speed and connectivity are crucial factors in both situations. Ethernet has been used for connecting devices in wired local area networks (LANs) and wide area networks for years (WAN). In order to divide the data stream into frames, devices connect across Ethernet. The source address, the destination address, and an error-checking system that guarantees proper transmission and reception are all contained in the frame. In order to provide a serial interface for exchanging control data between the Ethernet Media Access Controller (MAC) and the Physical Layer, control input and output interfaces are described in the IEEE802.3 standard. A device that manages MDIO and MDC is the Ethernet Management Interface Object. For design verification, semiconductor firms have created many approaches. Open Validation Methodology (OVM) and Universal Validation Methodology are both available (UVM). The Open Verification Methodology and several other approaches are the ancestors of the Universal Verification Methodology. A class library that supports robotization of the verification domain is part of the universal verification approach. System Verilog is used to create these class libraries. Simulators for the Hardware Description Language (HDL) and jobs for inspection in the Hardware Verification Language (HVL) are utilized in distinct ways. This HDL and HVL are combined into the Hardware Description Verification Language by System Verilog (HDVL). It integrates every design and validation element, including coverage, limited randomization, and assertion-based validation. The verification of a Wishbone bus-based MAC controller is addressed after the UVM verification technique is used to build a multi-level, reusable verification platform. This controller's system architecture blends original design parts with reused IP cores. Directed random test and assertion verification technologies are used to effectively complete the verification method.

II.DUT DESCRIPTION

2.1 Project Background

The Ethernet MAC Controller, a part of the proposed network processing system, is examined in this described system in terms of its implementation and verification. This PHY interface enables 10/100/1000 Mbps data transfer speeds with the additional PHY interfaces: an WISHBONE bus that provides 10/100/1000 Mbps data transfer rates; an IEEE 802.3-compliant GMII/MII interface to interact with an external Gigabit/Fast Ethernet PHY; and an alternative RGMII interface to interact with an external gigabit PHY. The Ethernet IP Verification System is proactively verified using a framework enabling layered, reusable verification that takes use of strategies like the assertion check method and constrained random data frame generation.

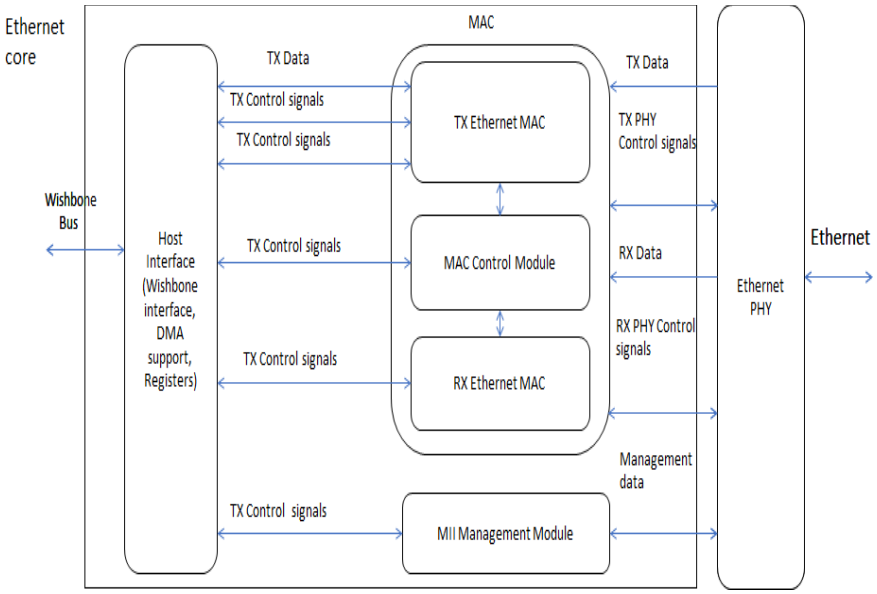

Figure 1: Ethernet MAC IP Core

2.2 Architecture Structure

The Ethernet IP Verification System consists of the WISHBONE bus and Ethernet MAC controller IP. The IEEE 802.3-compliant MAC controller is implemented by the Ethernet MAC. The MAC controller enables 10/100/1000 Mbps data speed using the IEEE 802.3- compliant GMII/MII PHY interfaces and features a WISHBONE bus interface. The two modules that make up the recommended environment are the transmitting module as well as the receiving module. Figure 2 displays the IEEE 802.3 data frame that consists of seven distinct fields. Earliest stages of frame delimiter, source and destination addresses, length, information, and frame check sequence are merged to form a single data frame that displays the seven fields.

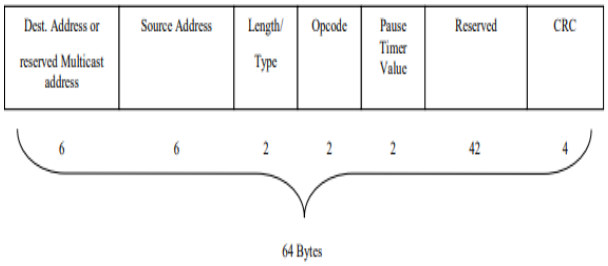

Figure 2: Ethernet frame Format

2.3 Wishbone Bus

The Wishbone bus is used to communicate with various devices. When developing SOCs, elastic interactions between different devices are critical to achieving maximum performance. Due to its open design and the large number of free Wishbone IP cores offered by the Open Cores Association, the Wishbone bus is used to communicate with a wide range of devices. Previously, IP cores were difficult to integrate using non-standard interconnection schemes. This required creating custom flash drive logic to pair each core together. By adopting a standard connection method, end users can connect cores quickly and easily. This pattern can be used for soft core, hard core or hard-core IP. WISHBONE interconnects are provided as universal interfaces. Thus, itdefines standard data exchange between basic IP modules.

The System-on-a-chip and design reuse are made easier thanks to the WISHBONE partnership, which establishes a uniform communication protocol. This technology has the following features:

1. A logical IP core hardware interface that isstraight forward and small and doesn't need a logic gate.
2. Encourages the use of structured design techniques by bigproject teams.

3. Full suite of well-known data bus protocols, including:
4. Read/write iterations
5. An operand size of up to 64 bits and a modular data bus.
6. Various core connection methods support point-to-point connection, common bus, and cross bus, switches and switch interconnects.
7. The handshake protocol allows each IP core to negotiate its data rate.
8. It supports data transmission in one cycle.

2.4 MAC Media Access Control Module

According to IEEE 802.3-2005A host's ability to transmit and receive information through Ethernet is made possible by the MAC Media Access Control module.

There are five modules in the Ethernet core:

a) The host interface utilises the WISHBONE to link the system's other components and the Ethernet Unit (using DMA transfers). Host interface also includes registers.
b) The TX Ethernet MAC carries out transmitting tasks.
c) The RX Ethernet MAC carries out receive tasks.
d) Full duplex flow control operations are carried out by the MAC Control Module.
e) The MII Management Module manages the PHY as well as gathers its information and updates.

The complete functionality of 10/100 Mbps Media Access Control is only possible while numerous modules are employed. Ethernet IP Component is based on the Carrier Sense Multiple Access / Collision Detection (CSMA/CD) standard and can function either in half-duplex or full-duplex mode. A station must monitor the activity on the media when it intends to transmit in half-duplex mode. Any station may begin transmitting when the media is idle. A collision on the media is noticed if there are two or more stations transmitting at the same moment. For an arbitrary period of time, all stations cease transmitting and withdraw. The station again monitors media activity after the back-off period. The medium begins broadcasting while it is not in use. The termination of the present transmission is anticipated by all other stations.

2.4.1 Host Interface

The host interface is connected to the RISC and memory using Wishbone. While using data frames to write to memory, the RISC automatically enters the information for the configuration registers. By using the DMA, it is feasible to get frames.

2.4.2 Transmit Ethernet MAC

The Transmit Ethernet MAC receives byte streams from the transmit logic, and in response generates 10BASE- T/100BASE-TX transmit MII nibble data streams (host). It carries out the required back-off and deferral procedures, controls the IPG, computes the checksum (FCS), and monitors the physical media (by monitoring Carrier Sense and collision signals).

2.4.3 Receive Ethernet MAC

The Receive Ethernet MAC interprets the 10BASE- T/100BASE-TX MII received data nibble streams and afterwards sends appropriately structured packet-byte streams towards the host. It examines the FCS, scans every packet for the SFD (start frame delimiter), examines about any dribbling nibbles, then verifies for received code infractions.

2.4.4 Medium Access Control Module

For the full-duplex operation, the Media Access Control block regulates real-time access. The station that is transmitting the packets can be stopped using the control opcode PAUSE. When the top layer is no longer able to accept incoming packets, the reception buffer (FIFO) fills up. A PAUSE control packet is sent by the top layer to the signal source just before an overflow. When the MAC Control module receives a PAUSE control packet, the information that was supplied to the pause timer value field is loaded into the pause timer. During the "pause timer value" slot periods, the Tx MAC is prevented from transmitting the packet data.

The following operations can be performed by the Media Access Control block:

i. Identification of control frames
ii. Creation of control frames
iii. Transmit/Receive MAC Interface
iv. Pause Timer
v. Slot Timer

III. VERIFICATION ENVIRONMENT

To test the functionality of the DUT, the stimulus is produced with the use of sequences. Sequencer refers to the block on which the sequences are initiated. Sequencers produce general sequences of data and transfer those sequences to another block known as driver, which handles communication with the DUT while being unaware of the communication bus. This block transfers the high-level class details to an interface block, which transforms them into low pin level information.

Although the driver keeps the DUT active by feeding it data produced by the sequencers, it doesn't validate the reactions to the stimuli. Another block is required that monitors and assesses the DUT's replies to the driver's communication. The monitor is this block. The inputs and outputs of the DUT are sampled by monitors. A predictor predicts the expected result. Monitor and predictor end their output to another block called the scoreboard, where it is compared and validated.

The UVM environment is created by these elements put together. A single agent is composed of sequencers, drivers, and monitors. Environmental components include an agent and a scoreboard. All of the test bench's blocks and sub blocks are under the control of the test block. This implies that we may add, delete, and override blocks in our test bench and produce alternative tests by simply altering a few lines of code rather than creating entirely new tests. This is made feasible via SV's support for OOPs.

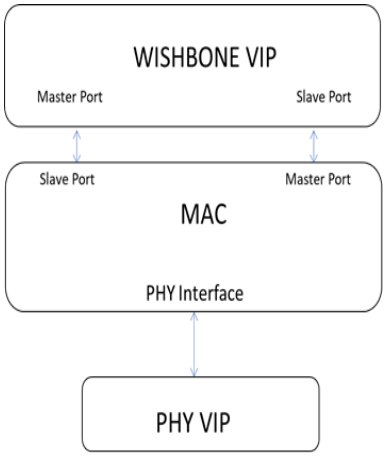

Figure 3: Ethernet IP Verification System Architecture

IV. VERIFICATION STRATEGY

The design has two sides, system and network with each of them having transmit and receive block. Each side of the design has the chain of PHY MII MAC blocks in TX & the reverse chain in RX. The chain joins the other side in the same pattern PHY MII MAC – MAC MII PHY. The same behavior is mimicked in the verification IP chain at both TX& RX ends. The DUT RX is connected to the VIP TX & vice versa. The VIP is an industry proven design of a similar chain and hence provides a reliable support in verifying the given design. Each block within the VIP has a separate driver and monitor which notifies in case of any error within the same. Before the normal operation of the DUT, all the blocks need to attain sync for which an idle setof data is sent along with the protocol headers. Both the DUT and the VIP need to acquire sync between their blocksbefore being score boarded for verification. The active monitor is the one that reads the data that is being driven intothe DUT while the passive monitor reads the data coming out of the DUT. Once, they are in sync, the data out of these two blocks are scoreboard and validated. Hence, based on UVM phases, a separate base test is written for each of them where the basic verifications are done. The specific scenario to be tested is generated by a separate test which derives the above and performs the additional functions required to generate the scenario and check the result. The concept of UVM phases ensures the interdependencies of the blocks are taken care. Thus, without disturbing the base structure, the same can be used to generate any number of new tests by using the concept of inheritance. All the basic configurations are made in the base tests and hence are visible to all the tests deriving the same.

V. TEST CASES

The following scenarios have been covered to test the functioning of the ETHERNET in accordance with thespecification: register reset, register write-read, Tx, Rx, and Tx-Rx flow control, collision detection and retransmission, back off algorithm. Valid data (Tx and Rx),the beginning and end of a packet, and the data included in the packets (Tx and Rx).

VI. RESULTS

In this Ethernet MAC IP, the provided input data is taken bymeans of WDATA channel of WISHBONE interface, then according to the mode & speed we select the frame will constructed and perform transmitting & receiving accordingly and finally we observe the output by means of RDATA channel of WISHBONE interface.

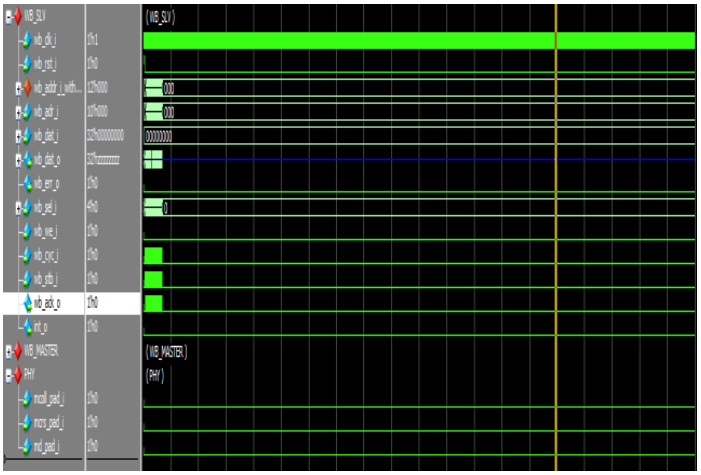

Figure 4: Reset all registers and read their values

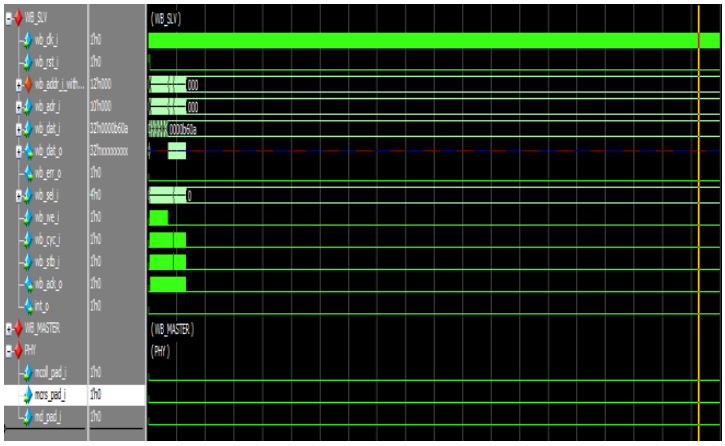

Figure 5: Read and Write Registers

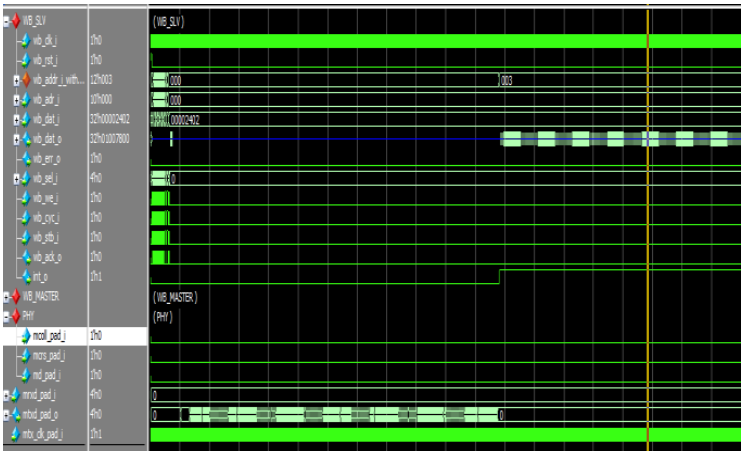

Figure 6: Transmit Data in Full Duplex Mode

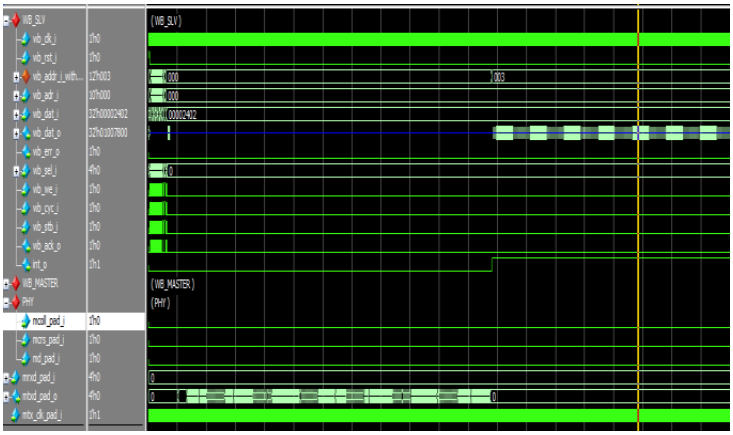

Figure 7: Receive Data in Full Duplex Mode

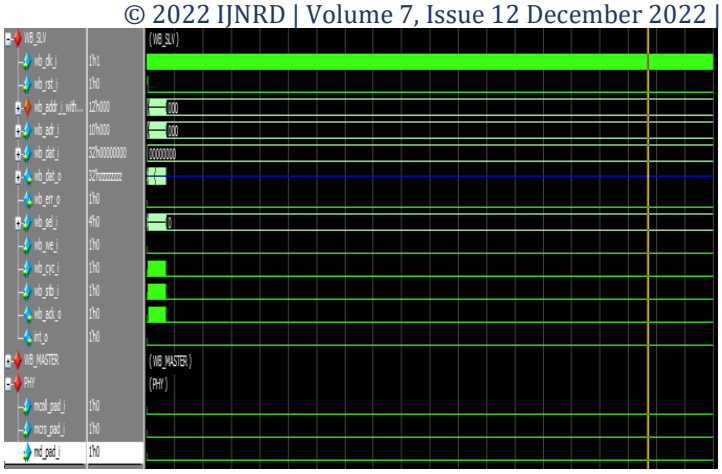

Figure 8: Half Duplex Mode of transmission

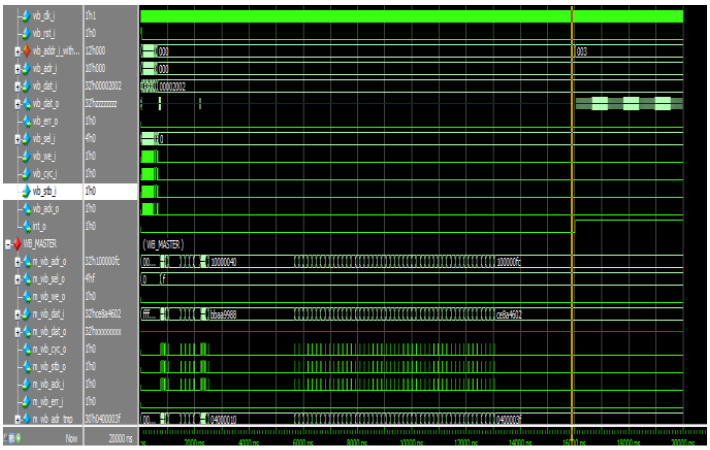

Figure 9: Collision detection and retransmission

VII. CONCLUSION

Verification is the most significant step in the product development process. One of the most well-known Verification Methodologies for verifying a complicated IP and SoC is Universal Verification Methodology (UVM). This article examines Ethernet and validates its protocol using test benches and standard testing formats. On the QuestaSim simulator, the UVM approach is successfully used to validate the Ethernet MAC requirements. An overview of the System Verilog and Universal Verification Methodology used to validate the Ethernet protocol is handed in this paper and can suitable to satisfy all of our calling criteria for the verification of this complex protocol by employing this strategy.

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