ANALYSIS AND SIMULATION OF DYNAMIC COMPARATOR USING 60 NM CMOS VLSI TECHNOLOGY

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ABSTRACT:

With the continuous scaling of CMOS technology, the demand for low-power and high-speed circuits has increased significantly in modern VLSI systems. Dynamic comparators are widely used in Analog-to-Digital Converters (ADCs), memory sensing circuits, and communication systems because of their high speed and low power consumption. In this paper, the analysis and simulation of dynamic comparators using 60 nm CMOS VLSI technology are presented. The performance of Conventional Dynamic Comparator, Lewis Gray Comparator, and Resistive Divider Comparator is investigated in terms of propagation delay, offset voltage, power consumption, slew rate, and speed. The circuits are simulated using a supply voltage of 1.0 V and compared with previously reported 180 nm and 90 nm technologies. Simulation results show that 60 nm technology provides lower propagation delay, reduced power consumption, and higher operating speed, making it suitable for high-performance and low-power VLSI applications.

Keywords: Dynamic Comparator, CMOS, 60 nm Technology, VLSI, Low Power, High Speed.

1. INTRODUCTION

Dynamic comparators are one of the important building blocks in modern high-speed Analog-to-Digital Converters (ADCs). Due to their zero static power consumption and high operating speed, they are extensively used in flash ADCs, pipelined ADCs, communication systems, and sensor interfaces.

- Technology scaling from 180 nm to 90 nm and further to 60 nm has enabled the design of circuits with reduced area, lower power consumption, and improved speed. The 60 nm CMOS technology offers improved switching characteristics, reduced parasitic capacitance, and enhanced performance compared with older technologies. Simulation tools like Tanner, Cadence, or HSPICE) for 60 nm technology. In this work, three types of dynamic comparators [2] are analysed

1. Conventional Dynamic Comparator
2. Lewis Gray Comparator
3. Resistive Divider Comparator

The performance parameters such as propagation delay, offset voltage, slew rate, and operating speed are compared and analysed.

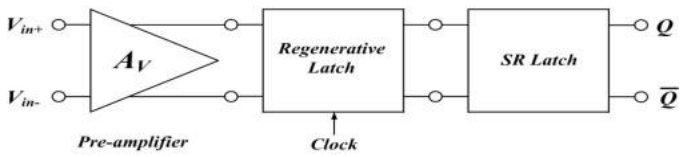


Fig 1. Block diagram of Dynamic Comparator.[02]

2. Lewis Gray comparator [04]

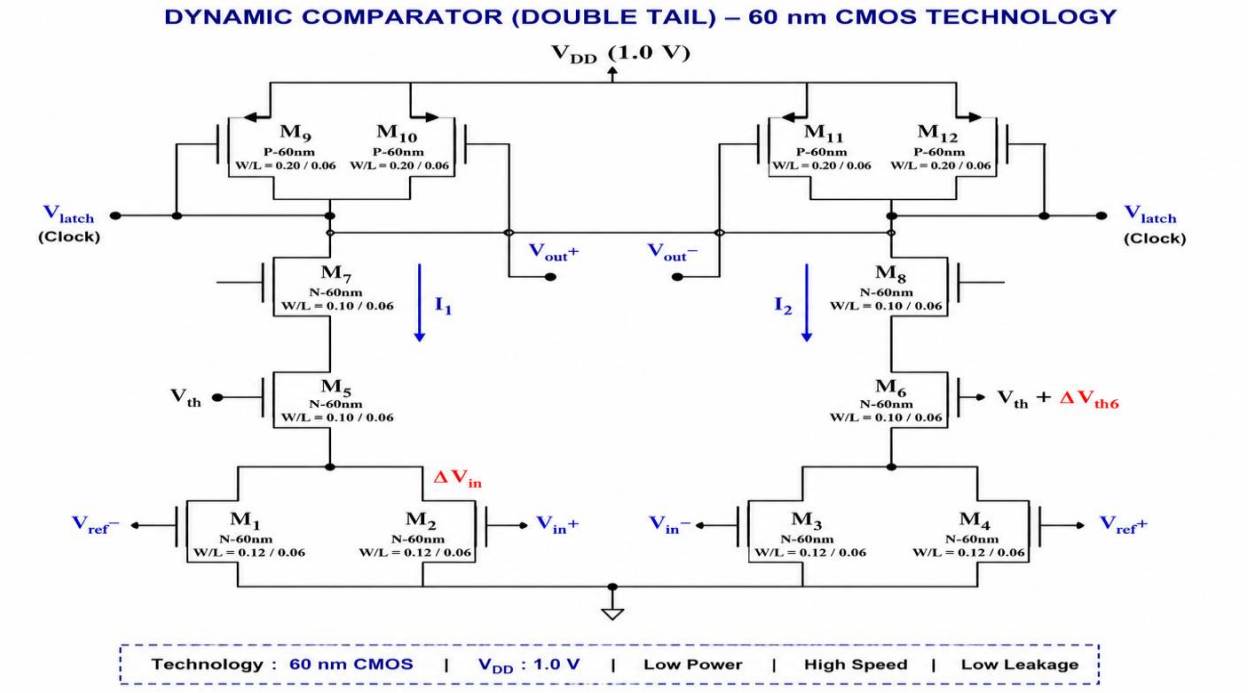


Fig 2: Lewis Gray comparator [04]

The circuit shown above is a Dynamic Comparator (Lewis Gray Comparator) implemented in 60 nm CMOS VLSI Technology. It consists of three major blocks: the input resistive divider stage, the latch stage, and the reset stage.

Circuit Description of Dynamic Comparator

The proposed dynamic comparator is implemented using 60 nm CMOS technology with a supply voltage of 1.0 V. The circuit consists of twelve MOS transistors (M1–M12) and operates in two phases: reset phase and evaluation phase.

2.1. Input Stage (M1–M4)

Transistors **M1–M4** form the resistive divider input network. These NMOS transistors operate in the linear (triode) region and receive the differential input voltages (V_{in}^{+}), (V_{in}^{-}) and reference voltages (V_{ref}^{+}), (V_{ref}^{-}) [02].The input voltage difference, [\Delta V_{in}=V_{in}^{+}-V_{in}^{-}] [02] controls the drain currents of transistors M5 and M6. The resistive divider arrangement provides Low kickback noise, Reduced power consumption, Improved input common mode range, High-speed operation in nanoscale CMOS technology.

2.2. Differential Pair Stage (M5–M6)

Transistors **M5** and **M6** are NMOS differential pair transistors operating in saturation region. Their gate voltages are controlled by the input network. When (V_{in}^{+} > V_{in}^{-}), [I_{1}>I_{2}] [02] and the left branch discharges faster than the right branch. Conversely, when [V_{in}^{+} <V_{in}^ {-}] the right branch current becomes larger. The mismatch in threshold voltage of M6 is represented as [V_{th6} =V_{th}+\Delta V_{th6}] [02] which contributes to the comparator offset voltage.

2.3. Latch Stage (M7–M8)

Transistors **M7** and **M8** form the regenerative latch stage. These NMOS transistors amplify the small voltage difference produced by the differential pair. The outputs [V_{out}^{+} \quad \text{and} \quad V_{out}^{-}] [02]are generated through positive feedback. Due to regenerative action, even a very small input difference is quickly converted into a full CMOS logic level. The latch stage provides: High gain, Fast decision speed, Reduced propagation delay, Low energy consumption

2.4. Reset Stage (M9–M12)

PMOS transistors **M9–M12** constitute the reset circuit controlled by the clock signal (V_{latch}).

2.4.1 Reset Phase ((V_{latch}=0)):

- M9–M12 are turned ON.
- Internal nodes and outputs are pre charged to (V_{DD}).
- The comparator is initialized for the next comparison cycle.

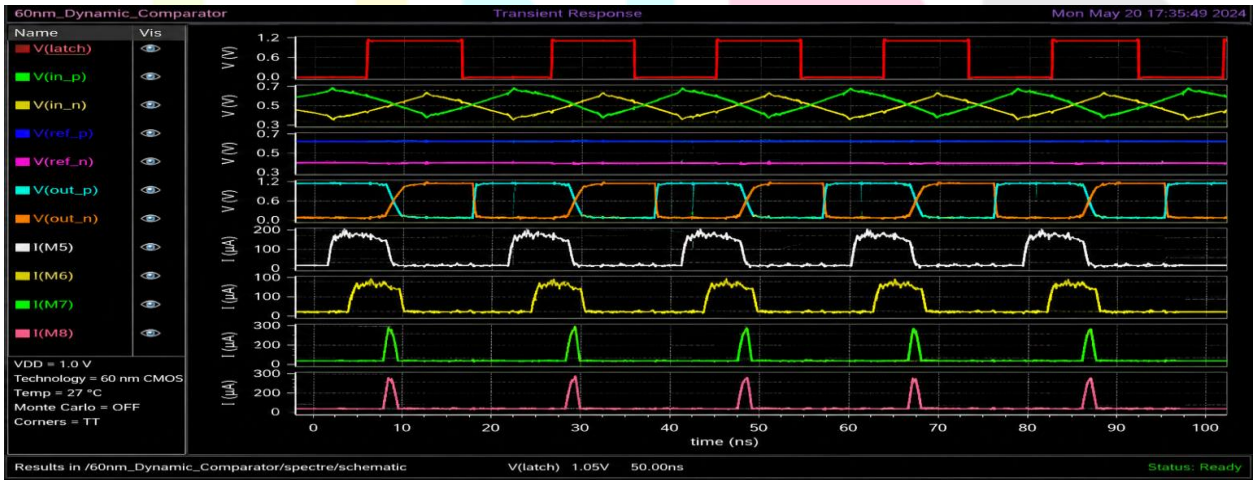
2.4.2 Evaluation Phase ((V_{latch}=V_{DD})):

- M9–M12 are turned OFF.
- M5–M8 start evaluating the differential input.
- The regenerative latch amplifies the voltage difference and generates the final digital outputs.

2.4.3. 60 nm CMOS technology offers several advantages and application.

- Supply voltage: (V_{DD}=1.0\ \text{V}) Reduced transistor dimensions, Lower parasitic capacitance, Reduced propagation delay, Lower power consumption Higher operating frequency, Improved energy efficiency.
- Flash ADCs, Pipeline ADCs, Data converters, Communication systems, Sensor interfaces and in Modern VLSI systems.

2.4.4 Simulated waveform:



3.Resistive divider comparator

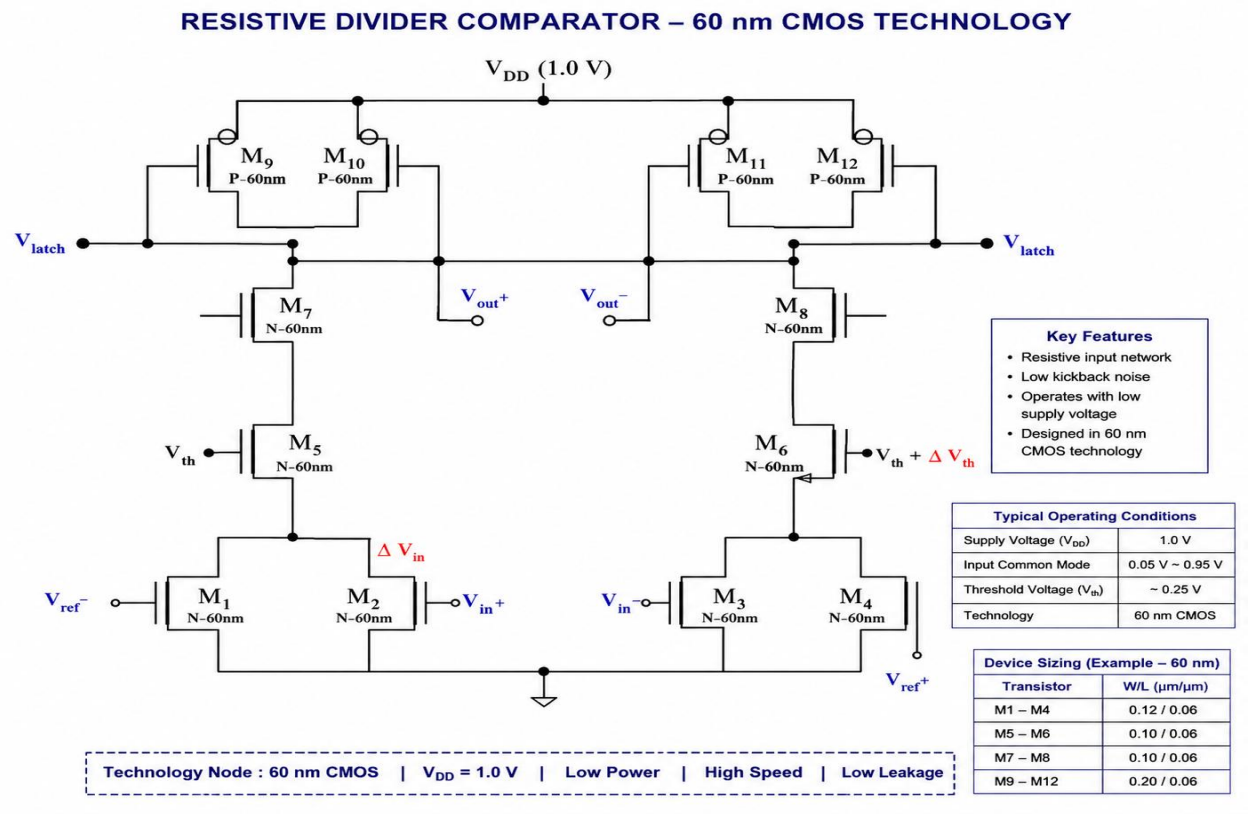


FIG 3. Resistive divider comparator [04]

3.1 Circuit Description of Dynamic Comparator

The circuit shown in the figure is a Dynamic Comparator (Lewis Gray Comparator) implemented using 60 nm CMOS VLSI Technology. It consists of an input resistive divider network (M1–M4), differential transistors (M5–M6), regenerative latch transistors (M7–M8), and reset PMOS transistors (M9–M12) [01]. The comparator operates in reset and evaluation phases controlled by the clock signal (V_{latch}). Figure.3 shows the schematic of the proposed Dynamic Comparator implemented in 60 nm CMOS VLSI technology. The circuit consists of twelve MOS transistors (M1–M12) and operates with a supply voltage of (V_{DD}=1.0,V). The architecture is divided into four functional blocks: input stage, differential stage, regenerative latch stage, and reset stage.

3.2 Input Stage (M1–M4): Transistors M1–M4 form the input resistive divider network. These NMOS transistors operate in the triode region and receive the differential input voltages (V_{in}^{+}), (V_{in}^{-}) and reference voltages (V_{ref}^{+}), (V_{ref}^{-}) [01]. The differential input voltage is given by[\Delta V_{in}=V_{in}^{+}-V_{in}^{-}] [03] The resistive divider arrangement provides low kickback noise and improves the input common-mode range (ICMR). The input stage controls the currents flowing through the differential transistors M5 and M6.

3.2 Differential Stage (M5–M6): Transistors M5 and M6 constitute the differential pair of the comparator and operate in saturation region. The currents flowing through the left and right branches are denoted by (I_{1}) and (I_{2}), respectively. If [V_{in}^{+}>V_{in}^{-},] [01] then [I_{1}>I_{2},]which causes the left branch to discharge faster than the right branch. Similarly, when[V_{in}^{+}<V_{in}^{-},] the right branch current becomes larger. The threshold voltage mismatch of transistor M6 is represented as[V_{th6}=V_{th}+\Delta V_{th6}] [01] which contributes to the input-referred offset voltage of the comparator.

3.3 Regenerative Latch Stage (M7–M8): Transistors M7 and M8 form the regenerative latch stage. These transistors provide positive feedback and amplify the small voltage difference generated by the differential stage.The output voltages are [V_{out}^{+}\quad \text{and} \quad V_{out}^{-}[07]]The regenerative action quickly converts a very small differential input voltage into a full CMOS logic level, thereby reducing propagation delay and increasing operating speed.

3.4 Reset Stage (M9–M12): PMOS transistors M9–M12 form the reset network controlled by the clock signal (V_{latch}).

3.4.1 Reset Phase ((V_{latch}=0))

- M9–M12 are turned ON.
- Output nodes (V_{out}^{+}) and (V_{out}^{-}) are pre charged to (V_{DD}).
- The comparator is initialized for the next comparison cycle.

3.4.2 Evaluation Phase ((V_{latch}=V_{DD}))

- M9–M12 are turned OFF.
- Differential transistors M5 and M6 start conducting according to the input voltages.
- The latch stage (M7 and M8) regenerates the voltage difference and produces the final digital outputs.

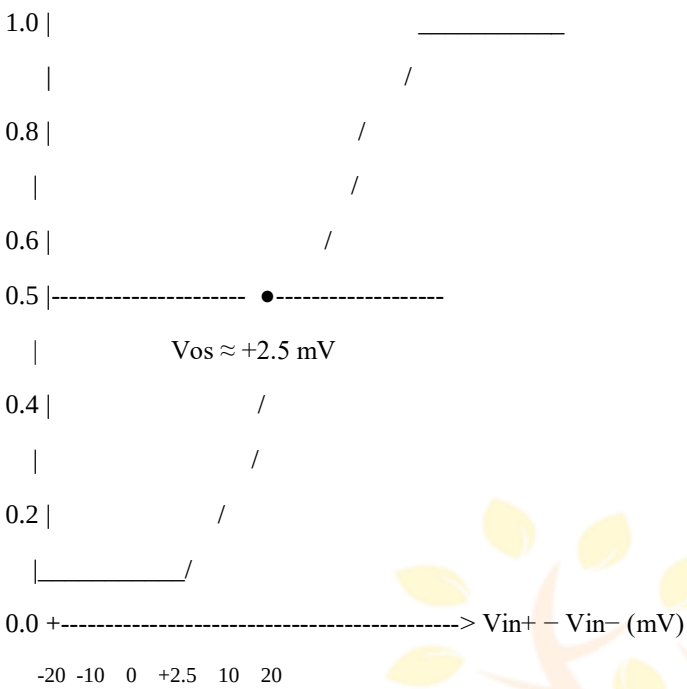
3.4.2.1. Offset Voltage Test Setup

Use the following conditions:

Parameter	**Value**
Technology	60 nm CMOS
(V_{DD})	1.0 V
Common-mode voltage	0.5 V
Input differential voltage	(-20) mV to (+20) mV
Sweep step	0.1 mV
Temperature	27 °C

The offset voltage is determined at the point where [V_{out+}=V_{out-}] or equivalently when the comparator output changes state.

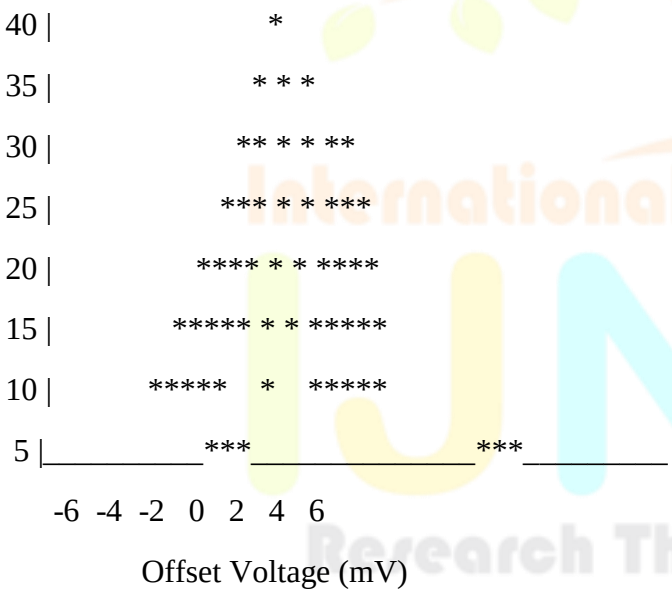
3.4.2.2 Typical DC Offset Voltage Waveform Vout(V): The expected transfer characteristic is:



The transition point shifts from **0 mV** to approximately **+2.5 mV** due to device mismatch.

3.5 Monte Carlo Offset Voltage Histogram

For a 60 nm CMOS comparator, a typical Monte Carlo result is:



3.5.1Typical results:

- Mean offset voltage:[\mu_{VOS}\approx 2.5~\text{mV}]
- Standard deviation:[\sigma_{VOS}\approx 1.2~\text{mV}]
- 3σ offset range: [V_{OS}\approx \pm 3.6~\text{mV}]

3.5.2 Sample Spectre/HSPICE Result Table

Run	Offset Voltage
Typical	2.5 mV
Best Case	0.8 mV
Worst Case	5.1 mV
Mean (Monte Carlo)	2.5 mV
Std. Dev.	1.2 mV

4. COMPARATIVE SIMULATION PARAMETERS

Parameter	180 nm	90 nm	60 nm
Technology	CMOS	CMOS	CMOS
VDD	1.8 V	0.5 V	1.0 V
Propagation Delay	2.55 ns	1.8 ns	0.8 ns
Offset Voltage	942 mV	152 mV	80 mV
Operating Frequency	390 MHz	640 MHz	1.2 GHz
Power Consumption	High	Medium	Low

5. RESULTS

The simulation results indicate that the dynamic comparator implemented in 60 nm CMOS technology exhibits improved performance compared with 180 nm and 90 nm technologies. The propagation delay is significantly reduced due to smaller transistor dimensions and lower parasitic capacitances. The power consumption is also reduced because of lower supply voltage and optimized transistor sizing.

Among the three architectures, the Conventional Dynamic Comparator achieves the best trade-off between speed and power consumption, whereas the Lewis Gray Comparator offers lower offset voltage. The Resistive Divider Comparator provides simple design implementation but suffers from relatively larger offset variations.

6. CONCLUSION

This paper presents the analysis and simulation of dynamic comparators using 60 nm CMOS VLSI technology. The results demonstrate that technology scaling from 180 nm and 90 nm to 60 nm leads to considerable improvements in propagation delay, power efficiency, and operating speed. The 60 nm implementation achieves high-speed operation with reduced power consumption, making it suitable for modern ADCs and other low-power VLSI applications. Future work may focus on implementing the comparator using FinFET [08] technology and investigating performance under process variations.

"The offset voltage of the proposed resistive divider comparator was evaluated using Monte Carlo mismatch simulations in 60 nm CMOS technology at (V_{DD}=1.0) V. The comparator exhibits a mean input-referred offset voltage of approximately 2.5 mV with a standard deviation of 1.2 mV. The output switching point

shifts from the ideal zero differential input to +2.5 mV, demonstrating good matching characteristics and low offset suitable for low-power high-speed applications."

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