COMPARATIVE ANALYSIS OF CMOS AND ADIABATIC ECRL CIRCUITS

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Abstract— Power consumption is of utmost importance in the field of semiconductor industry. Several techniques have been employed to reduce the power consumption in the electronic devices one of which is the adiabatic logic. There are two types of adiabatic circuits, partially adiabatic and fully adiabatic circuits. In this thesis work we have used partially adiabatic circuits. Positive Feedback Adiabatic Logic and Efficient Charge Recovery logic (ECRL) are the two prominent partially adiabatic logic styles. Several circuits were implemented using conventional CMOS and adiabatic ECRL logic and the performance of the circuits is compared in terms of power consumption, delay and transistor count. It is found that there is a significant difference in the parameters compared. The circuits are implemented in cadence virtuoso 6.1.5 and simulation is carried out in spectre MMSIM131.

Index Terms— Adiabatic logic, Partially adiabatic, Fully adiabatic, PFAL, ECRL

I. INTRODUCTION

The need for reduced power dissipation in the electronic devices is increasing day by day. This is the era of portable devices. But these portable devices come with a constraint in battery life. This is the main drawback of these devices and a challenging issue to the semiconductor industry. Battery life is now a product differentiator in many systems. Since today's ICs work at a very high speed there is more switching activity. The consequence of this increased switching activity is the increase in power dissipation which demands the need for cooling systems in the device which makes it bulky. Several methods have been employed to address the issue of power consumption. Commonly used method was scaling the supply voltage [1]. But supply voltage scaling has a negative effect in the performance of the circuit. Recently new techniques have been developed which reduce the power dissipation without altering the performance of the circuit. Adiabatic technique is one such promising method which guarantees a significant reduction in the power consumption. They work on the principle of adiabatic charging and discharging in which the energy is recycled from the output node instead of discharging it to the ground. Adiabatic logic family has many methods such as PFAL, ECRL, 2N2NP etc. In this paper, 2:1 MUX, 4:1 MUX and 8:1 MUX circuits are simulated using both conventional CMOS and adiabatic ECRL logic and the results of both the methods are compared with each other.

II. CMOS LOGIC

Fig 1 shows the charging and discharging process in conventional CMOS circuits. Conventional CMOS circuits achieve a logic '1' by charging the load capacitor to supply voltage Vdd and logic '0' by discharging it to ground [2]. Power dissipation in CMOS logic is caused by the switching activity of the device. The power consumed by the CMOS circuit can be divided into two major classes static and dynamic.

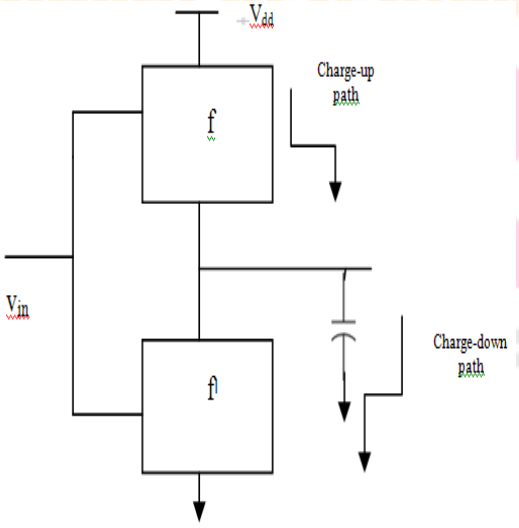

Figure 1: charging and discharging process in CMOS logic

The static power dissipation depends on the logical state of the circuit where as the dynamic power dissipation depends upon the switching activity of the device. Static power dissipation is given by

$$P_{static} = I_{static} V_{DD} \quad \text{---- (1)}$$

Where Istatic is the current through the circuit when there is no switching activity.
Dynamic power dissipation occurs when there is switching activity in the circuit. It is given by

$$P_{dyn} = CV_{DD}^2 f \quad \text{---- (2)}$$

Where C is the load capacitance and f is the clock frequency.

III. ADIABATIC LOGIC

In adiabatic circuits the heat is not dissipated to the ground because the energy is recycled in this logic. Hence there will be no exchange of heat with the environment. In traditional CMOS circuits the load capacitances are discharged to ground wasting the energy. But in adiabatic circuits the output load is reused thus saving the energy. Fig.2 shows the charging and discharging process in adiabatic circuit.

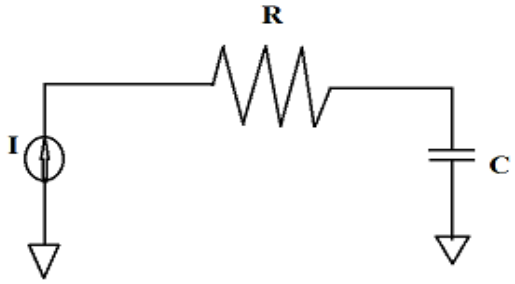

Figure 2: Adiabatic logic

In adiabatic circuits a time varying voltage source is used instead of a constant voltage supply. Therefore there will be great decrease in the current and hence the overall power dissipation in this logic will be reduced to

$$P = \frac{RC}{T} * CV_{DD}^2 \qquad \text{---- (3)}$$

Adiabatic logic can be classified into two main categories as fully adiabatic circuits and partially (quasi) adiabatic circuits. In fully adiabatic circuits all the charge that is stored in the load capacitance is fed back to the power supply hence making the circuits slower. Pass Transistor Adiabatic Logic (PAL), and Split-Rail Charge Recovery Logic (SCRL) are the two most popular fully adiabatic logic circuits. In partially adiabatic circuits some charge is allowed to be transferred to the ground. i.e. some heat is dissipated. But these circuits are easy to implement compared to fully adiabatic circuits. Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL) are the commonly used partially adiabatic logic circuits.

Efficient charge recovery logic (ECRL)

ECRL logic is an ideal logic for low energy systems. Cross-coupled PMOS transistors are used in ECRL logic. The generalized logic block of ECRL is shown in figure 3. It consists of two cross-coupled transistors M1 and M2 and two N-functional blocks. Power clock is used here to reuse the supplied energy. Both out and outbar are generated [3].

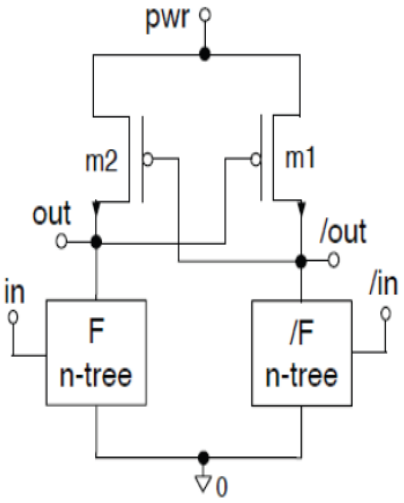

Figure 3: Adiabatic ECRL logic

IV. CIRCUITS AND SIMULATION

In this section we examine the behavior of various circuits (2:1 MUX, 4:1 MUX AND 8:1 MUX). These circuits are designed and simulated in both conventional CMOS and ECRL logic style. The results of both the logic styles are compared with each other. The parameters like power consumption, delay and transistor count are used for comparison. Circuit implementation is done in cadence virtuoso 6.1.5 and simulation is performed using spectre MMSIM131.

A multiplexer (or mux) is a device that acts as control switch. A generalized block diagram of a 2:1 mux is shown below fig 4. It has two input data lines I_0 and I_1 and a select line sel. This can be equated to a control switch as show below.

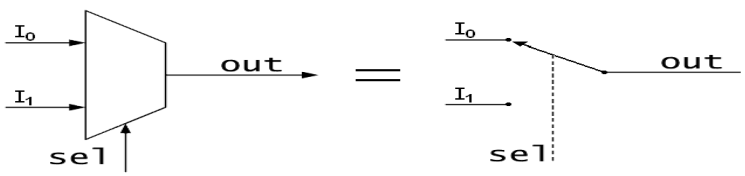

Figure 4: general block diagram of a 2:1 mux

Table 1: Truth table of a 2:1 mux

S	I_0	I_1	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Boolean expression= $I_0 \overline{S} + I_1 S$

The below figures show the implementation and simulated output of the circuits.

2:1 MUX:

The below fig.5 shows the schematic of CMOS 2:1 mux. NAND and inverter blocks are implemented first and 2:1 mux is implemented using those blocks.

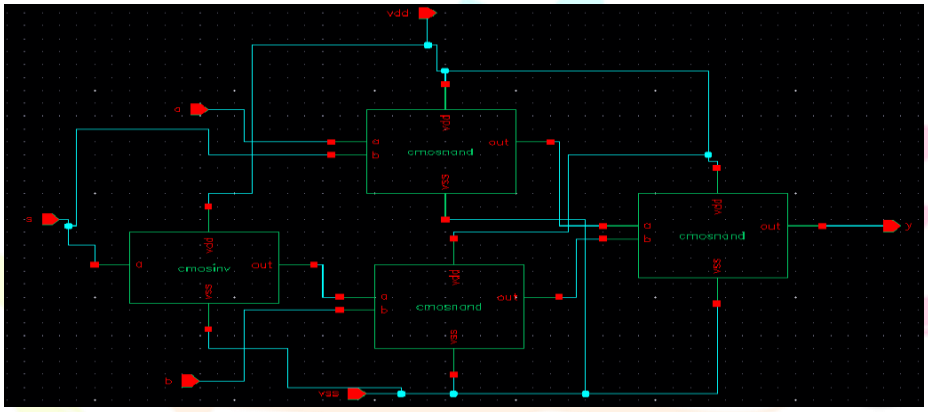

Figure 5: Schematic of CMOS 2:1 mux

Fig.6 shows the simulated output of the circuit. The first two waveforms are the inputs; third waveform is the output waveform which depends upon the select line. i.e., when the select line is 0 first input is selected and when the select line is 1 second input is selected and the corresponding output is generated.

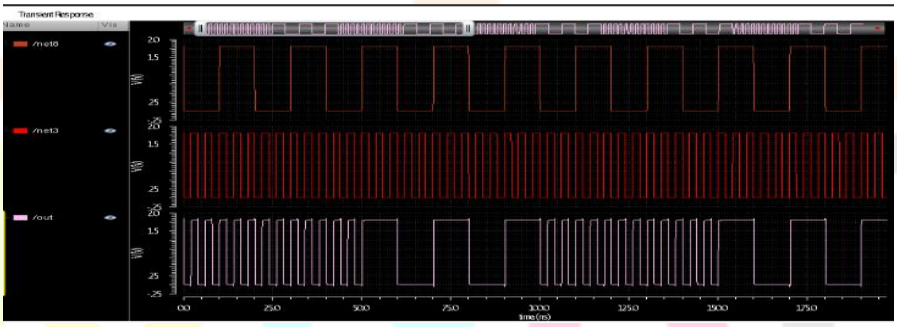

Figure 6: Simulated output of CMOS 2:1 mux

Fig.7 shows the schematic of ECRL 2:1 mux.

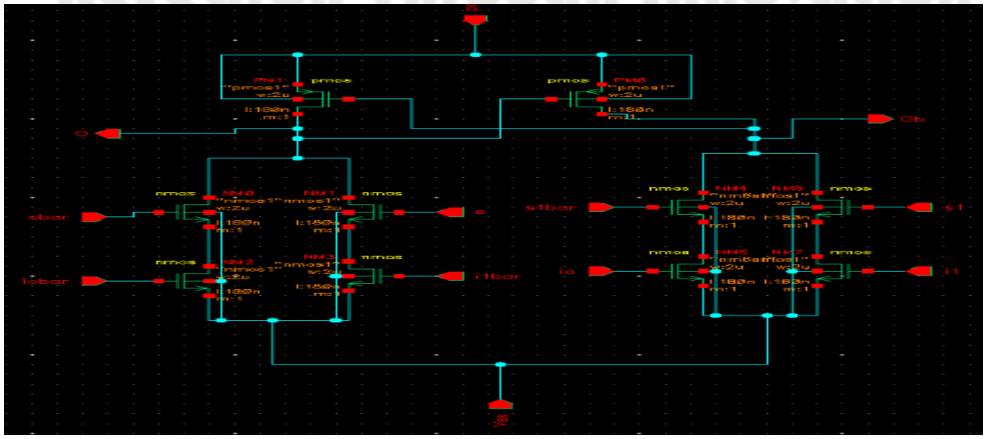

Figure 7: Schematic of ECRL 2:1 mux

Fig.7 shows the simulated out of the circuit. Here out as well as outbar are generated. The first waveform is the output waveform and the second waveform is the outbar waveform. Fourth and fifth waveforms are the inputs and the last waveform is the select line.

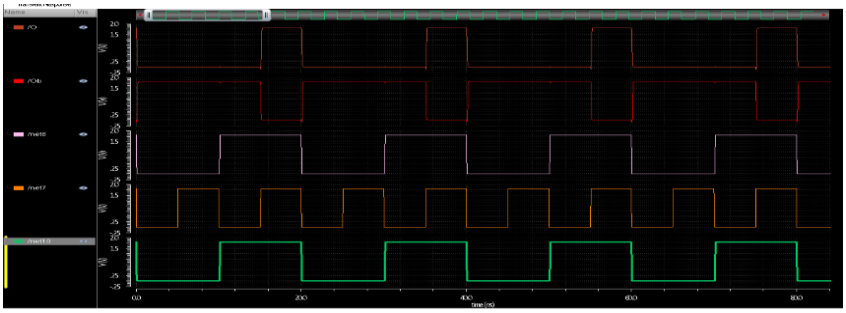

Figure 8: Simulated output of ECRL 2:1 mux

4:1 MUX:

Fig.9 shows the schematic of CMOS 4:1 mux which is implemented using 2:1 mux.

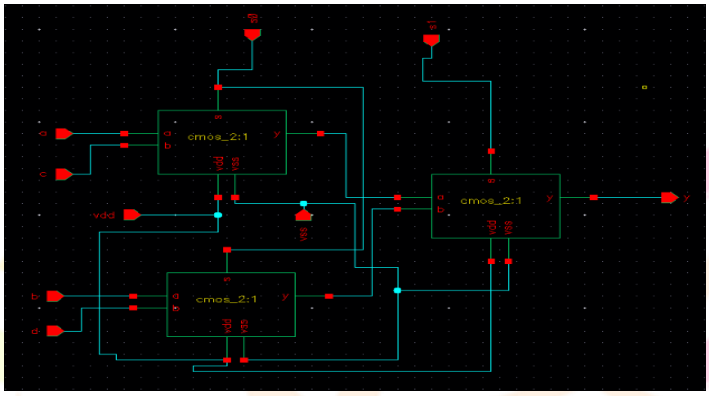

Figure 9: Schematic of CMOS 4:1 mux

Fig. 10 shows the simulated output of the circuit. First four waveforms are the input waveforms. Fourth and fifth waveforms are the two select lines and the last waveform is the output waveform. Depending upon the states of the two select lines inputs are selected and the corresponding output is generated.

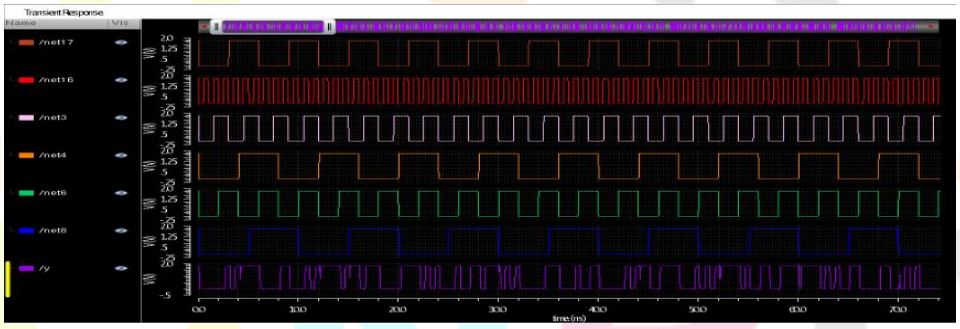

Figure 10: Simulated output of CMOS 4:1 mux

Fig 11 shows the schematic of ECRL 4:1 mux.

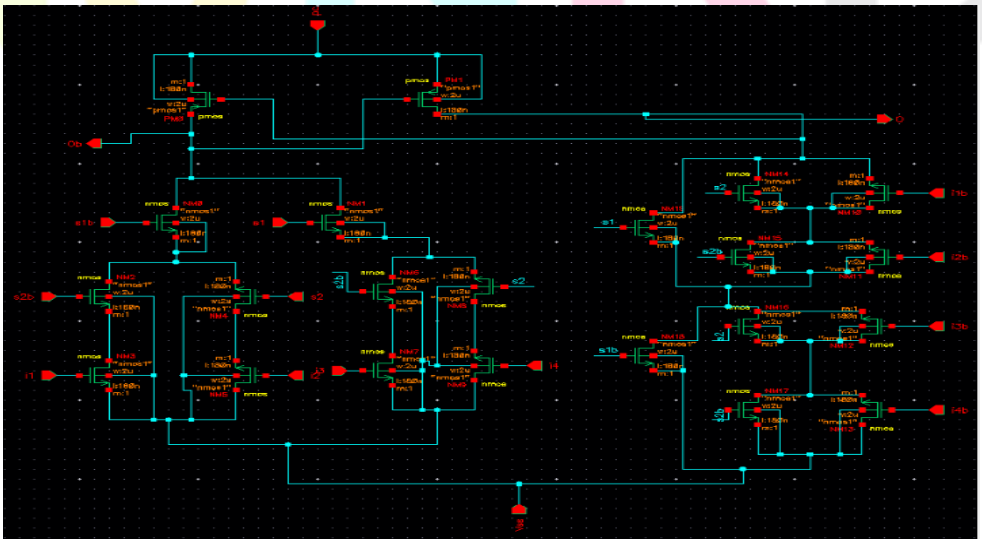

Figure 11: Schematic of ECRL 4:1 mux

Fig.11 shows the simulated output of the circuit. Here the first two waveforms are the select lines. Next four waveforms are the input waveforms. Last two waveforms are out and outbar respectively.

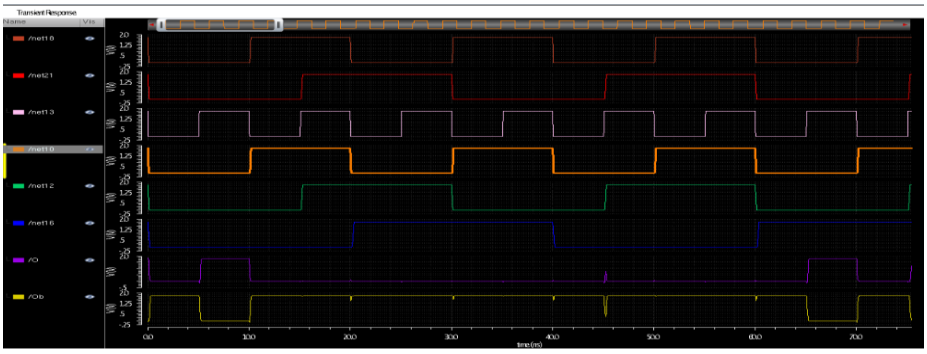

Figure 12: Simulated output of ECRL 4:1 mux

8:1 MUX:

Fig 13 shows the schematic of the CMOS 8:1 mux whch is implemented using two 4:1 mux and a 2:1 mux .

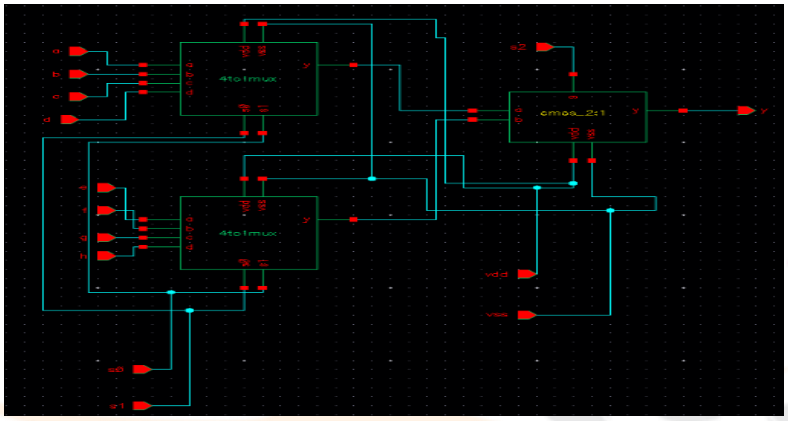

Figure 13: Schematic of CMOS 8:1 mux

Fig.14 shows the simulated output of the circuit. Here four select lines are used. Here the first eight waveforms correspond to the input waveforms and the next four waveforms are the select line waveforms and the last one is the output waveform.

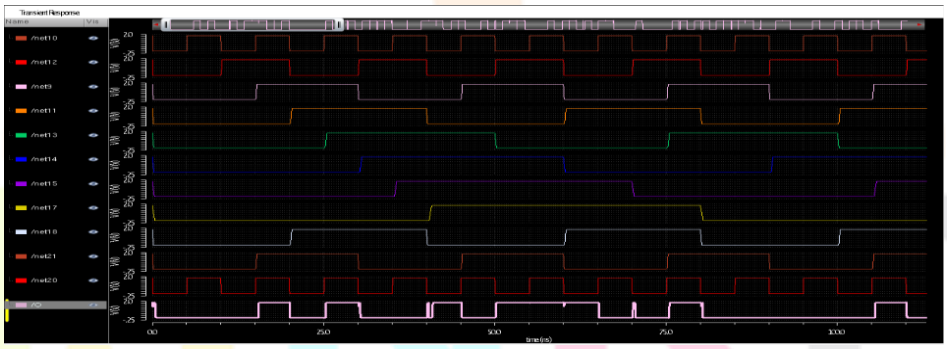

Figure 14: Simulated output of CMOS 8:1 mux

Fig.15 shows the schematic of ECRL 8:1 mux which is implemented using two 4:1 mux and a 2:1 mux.

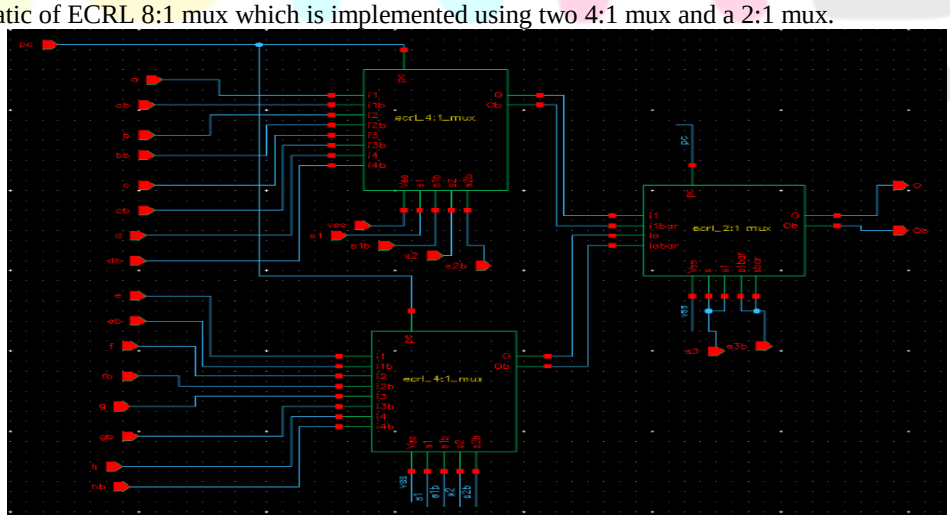

Figure 15: Schematic of ECRL 8:1 mux

Fig 16 shows the simulated output of the circuit. The first eight waveforms are the input waveforms, next four waveforms are the select lines and the last two waveforms are the out and outbar respectively.

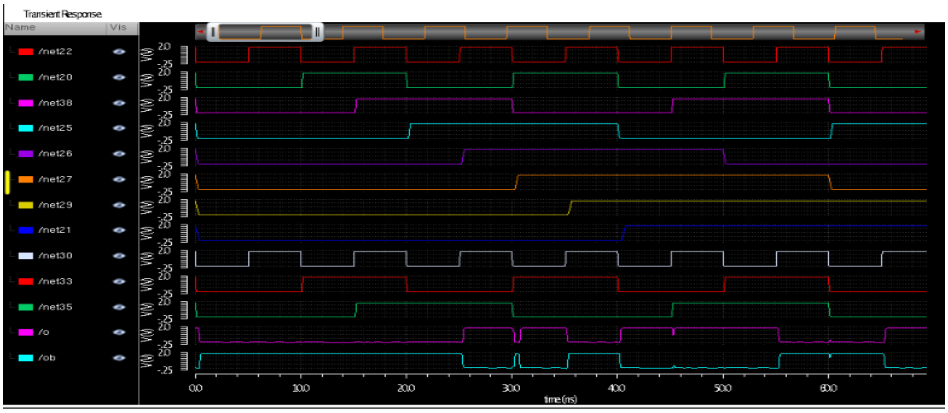

Figure 16: Simulated output of ECRL 4:1 mux

V. RESULTS AND CONCLUSION

The below tables show the obtained results.

Table 2: 2:1 mux

Logic/Parameter	Power Dissipation(µW)	Delay(nS)	Transistor count
CMOS	2.234	0.182	14
ECRL	1.07	0.057	10

Table 3: 4:1 mux

Logic/Parameter	Power Dissipation(µW)	Delay(nS)	Transistor count
CMOS	2.50	0.207	42
ECRL	1.668	0.03	22

Table 4: 8:1 mux

Logic/Parameter	Power Dissipation(µW)	Delay(nS)	Transistor count
CMOS	2.727	0.212	98
ECRL	0.863	0.163	54

The above results show us that ECRL logic greatly reduces the power dissipation in the circuits without any change in the performance of the circuit.. Upto 70% reduction in the power dissipation is observed. Delay is also reduced almost upto 80% and the transistor count is also reduced upto 50%. We can say that adiabatic ECRL logic is a better choice when compared to conventional CMOS logic.

There is an energy loss observed in adiabatic circuits too which is called as adiabatic energy loss. This occurs mainly because only some part of the output load capacitance is reused. To avoid this loss fully adiabatic circuits can be used which reuse the entire load capacitance but at the cost of circuit complexity.

VI. ACKNOWLEDGMENT

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